

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Guy B. Irving et al.  
Serial No.: 08/848,816  
Filing Date: May 4, 2001  
Group Art Unit: 2111  
Examiner: Khanh Nmn Dang  
Title: **SERVER CHASSIS HARDWARE MASTER  
SYSTEM AND METHOD**

**MAIL STOP AMENDMENT**

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

**DECLARATION PURSUANT TO 37 C.F.R. § 1.131**

I, the undersigned, hereby declare and state that:

1. I am over the age of 21 years, of sound mind, and competent in all respects to make this Declaration.

2. I am an inventor of the subject matter of the above-referenced patent application, entitled *Server Chassis Hardware Master System and Method*, filed on May 4, 2001 (the "Application").

3. I was employed by Anigma, Inc. ("Anigma"), which was hired by RLX Technologies, Inc., the assignee of the Application (the "Assignee"), prior to July 12, 2000, to perform services related to a project entitled RLX Orbiter (the "Project"). As an employee of Anigma, I performed tasks relating to the Project and worked closely with employees of the Assignee.

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4. During the performance of my duties relating to the Project and prior to July 12, 2000, Guy B. Irving and I (the "Inventors") conceived the subject matter of at least Claims 1, 9, 10, 13, and 16 of the Application (the "Invention").

5. Beginning after conception of the Invention and prior to July 12, 2000, I participated in the design and creation of a single board server assembly and master circuitry program that incorporated the subject matter of the Invention. The single board server assembly and master circuitry program resulted in the completion of a prototype. The design and creation of the single board server assembly and master circuitry program and the completion of the prototype were ongoing endeavors to which I devoted a substantial portion of business hours beginning on a date before July 12, 2000 and continuing at least through July 23, 2000. The conception of the invention is further evidenced by a Specification entitled "Firmware Interface Specification Orbiter 1680, Orbiter 3360" that describes the subject matter of the invention, attached hereto as Exhibit A. The date of the Specification, which has been redacted for privacy reasons, is prior to July 12, 2000.

6. During the construction of the prototype, at least six versions of design schematics were completed before July 12, 2000, and included embodiments of the Invention. Attached as Exhibits B and C, respectively, are fifth and sixth versions of design schematics. The dates of the design schematics, which have been redacted for privacy reasons, are prior to July 12, 2000. The design schematics are each twenty-seven pages long and illustrate the complexity of the construction of the prototype.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. Further, I declare that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

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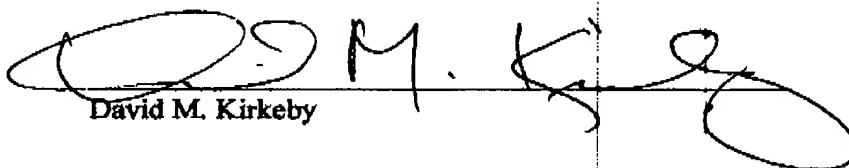
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PATENT APPLICATION  
09/848,816

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Declaration pursuant to 37 C.F.R. § 1.131 in regard to 09/848,816.

Signed this 4 day of MARCH, 2005.

  
David M. Kirkeby

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**EXHIBIT A**

# Firmware Interface Specification

## Orbiter 1680, Orbiter 3360

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## **1. SCOPE**

This document defines the interface to the Orbiter devices that are accessible and or controllable by firmware or software.

This document also defines the operation of the BIOS that is unique to the Orbiter.

## **2. OVERVIEW**

The Orbiter is a single board server. Up to two 2.5 inch hard drives or one 3.5 inch hard drive can be installed on the Orbiter PCBA.

Up to 24 Orbiters can be installed in a single specially designed enclosure (the HotDock Chassis).

The Orbiter uses a Transmeta processor (either the 3200 or the 5400). The Transmeta processors execute x86 type instructions. The Orbiter is a PC compatible type computer and most of the software interface on the Orbiter is compatible with standard PC design. The Orbiter includes some system monitoring and control devices that are not part of the standard PC architecture. The function of these devices and the interface to them are defined in detail in this document.

## **3. BIOS DESIGN**

### **3.1. Original BIOS**

The Orbiter BIOS is derived from the Phoenix ??? BIOS. This BIOS is a standard PC BIOS designed to run with the Transmeta 5400 and 3200 processors. This BIOS supports all current standard PC BIOS functionality including the following:

- Support for UltraDMA 66 IDE interface
- Support for boot from CD

### **3.2. Standard Features Not Part of Orbiter**

The following devices are not part of the Orbiter. The BIOS may, but need not be designed to support these devices:

- Parallel Port
- USB Port
- Audio Codec
- Beeper
- Floppy Disk

### **3.3. Redirection of Display Output to Serial Port 1**

The Orbiter BIOS redirects display I/O to serial port 1 when a display adapter is not detected. The default setup for Serial port 1 and serial port 2 is 38,400, 8 bits, no parity and no flow control.

### **3.4. LED indicators**

The POST code results are displayed by blinking the Board Fault LED and Front Panel LED. The board good LED is turned on if the BIOS does not detect any problems. See the GPIO Output section for more details on the function of these LED's

### **3.5. LM87 Support**

The Orbiter uses a National Semiconductor LM87 to monitor environmental status including voltages, fans and temperatures.

The BIOS sets up the LM87 limit registers as defined in this document so as to generate an SMB alert when a monitored parameter is out of range.

The BIOS loads status obtained from the LM87 into an extended DMI table.

The BIOS provides a mechanism for an external program to cause a DMI table refresh.

### **3.6. GPIO Table setup**

Much of the South Bridge I/O has been redefined to support system monitor and control functionality. The BIOS provides the following functionality with regard to the GPIO ports.

- Sets up the ALI1535 I/O appropriately for the Orbiter functionality. See the GPIO Assignments for RLXORB section for details on the set up of the GPIO tables.
- Provides a call to allow the state of the input to a GPIO device used as an input to be determined.
- Provides a call to allow the state of the GPIO output to be set for a device used as an output.
- Provides a call to allow the interrupt generated by a GPIO to be hooked.

The GPIO port to be activated is referenced by its port number and not its function in the BIOS calls.

### **3.7.SMB Bus**

The Orbiter SMB bus can access local SMB devices and System SMB devices. See the SMB (I<sup>2</sup>C) Bus Addressing section for the addresses of the I<sup>2</sup>C.

The Orbiter selects between the local and the system SMB bus using the signal, LOCAL\_I2C\_SEL. See the GPIO Assignments for RLXORB for details on this signal.

The BIOS provides access to the I<sup>2</sup>C bus via a call.



All installed Orbiters can have access to the system I<sup>2</sup>C bus. It is therefore necessary that this bus be accessed using I<sup>2</sup>C multi-mastering techniques. It is desirable that if the system I<sup>2</sup>C bus is busy that the Orbiter reselect the local I<sup>2</sup>C bus and wait about a millisecond before retrying the bus. This procedure will reduce the capacitive loading on the I<sup>2</sup>C bus which will improve the reliability of communication on the system I<sup>2</sup>C bus. It would also be desirable that a small additional time be added to the wait time based on the card slot. This procedure will eliminate the possibility of two devices preventing access for each other.

### 3.8. Watchdog timer

The ALI1535 contains a watchdog timer. The BIOS provides the hooks to enable the watchdog timer. The resident management program handles the watchdog timer if it is enabled to do so. The BIOS provides access to the environment monitor circuits by extending the DMI interface. In addition, the BIOS is extended to include support for a few control functions.

## 4. OVERVIEW GPIO INPUTS AND OUTPUTS

### 4.1. Inputs

Item	Description
Slot ID	6 bit code that indicates what slot this card is installed in
Power Supply Status	10 status lines (5 from each power supply) that indicates power supply status. See the Power Supply Status Lines section for more details on these signals.
Master/non-Master	A single GPIO input that indicates whether this card is installed in the master slot and therefore has master capability or not. See the Master Signal Function section for more details on the function of this signal.
Front Panel System Fault LED Control	The front panel system fault indicator enable line
Front Panel Board Fault LED Control	The front panel Orbiter board fault indicator enable line

### 4.2. GPIO Outputs (Excluding System Command Bus)

Item	Description
Board Fault LED (BRD FAULT LED)	Controls the state of the local board fault LED and the global board fault LED signal.
Board Good LED (BRD GD LED)	Controls the state of the board good LED.
Front Panel LED (ORB LED)	Controls the state of the front panel LED for this board.
Fan High (FAN HI)	Controls the high fan speed request line for this board.
Flash Write Enable (FLASHWE#)	Enables writing of the flash

#### 4.3. System Command Bus

The Orbiter in the master slot can control the System Command Bus. The System Command Bus allows the Orbiter installed in the Master slot to send various commands to any other Orbiter.

The signals of this bus are as follows:

Item	Description
Slot Address (MBADD0_OUT to MBADD5_OUT)	This is the 6 bit address of the slot that the command is targeted for
Command (MBCMD0_OUT to MBCMD2_OUT)	This is a three bit bus that defines the command to be executed
Strobe (MBSTROBE_OUT#)	When this signal is driven low the targeted Orbiter executes the command. The strobe must be returned to a high to allow command completion

The commands are as follows:

Command	Description
000	Nothing happens. Intentionally left as a no op to reduce possibility of an unintentional command
001	Causes a reset on targeted card
010	Causes the password interrupt line to be strobed
011	Causes a reset with CMDBUS_EVNT set
100	Cause the TST_BRD_PRES_IN# signal to go low
100 thru 111	Nothing happens. Reserved for future expansion

#### 5. MASTER SLOT SIGNAL

Each Orbiter has an input pin that indicates if it is the “Master Computer”. A computer that is the “Master” differs from all other Computers installed in the HotDock Chassis as follows:

- The System command bus is enabled to function for that computer.
- The Master input to the Master GPIO is high. This allows the system application to detect this and assign extended functionality to the “Master” computer.

The MASTER signal is high for only one device in the HotDock chassis. The logic for determining which device is “Master” is as follows:

- MASTER is always low for slots 3 through 24
- MASTER is always low for slots 1 and 2 if a Shelf Management Controller (SMC) is installed.
- MASTER is high for slot 1 if an SMC is not installed.
- MASTER is high for slot 2 if an SMC and a card in slot 1 is not installed.

#### 6. RAM SIZING

There is no on board RAM. All RAM is in a single DIMM. The BIOS needs to poll this DIMM and set the RAM size appropriately.

## 7. CMS STORAGE

Transmeta recommends that the CMS code be stored in the BIOS ROM for production. Are there any Phoenix issues with this? Will RocketLogix handle the development of the binary BIOS image?

## 8. FAN SPEED CONTROL

Fan speed control will be implemented with a resident management program that polls the temperature inputs and determines whether it is safe to operate this card with a lower fan speed. If the resident management determines that it is safe the resident management program can set FAN\_HI low. If all installed Orbiters set FAN\_HI low the fan speed will be reduced to medium speed, otherwise the fan speed will be high.

## 9. POWER STATUS LINES

Each of the two power supplies has five status outputs. The definition of these status lines is:

Item	Description
PWOK	All DC outputs are within tolerance PWOK=HIGH indicates power OK This signal drives system fault LED control via an isolating diode.
ACOK#	AC input power is within expected range. A jumper on the LED board is installed to set the expected range to 200 to 240 VAC. If the jumper is not installed the expected range is 100 to 240 VAC. ACOK#=LOW indicates AC is ok
FAIL	A power supply failure has occurred. FAIL=HIGH power supply failure including fan has occurred.
PRFL	A power supply failure is predicted PRFL = HIGH indicates power supply is failing, Fan may not be functioning properly
PRESENT#	The power supply is present PRESENT#=LOW indicates supply is present

## 10. LM87 INFORMATION

### 10.1. LM87 Input Description

Item	Description
Fan Monitor	The tachometer output of the fan that is mounted in front of this Orbiter. Four slots share the same fan tachometer input.
Voltage	The voltage status of the LM87 for the CPU core voltage, 3.3 volts, 5 volts and 12 volts. The 2.5 volts is monitored via a general purpose analog input of the LM87.

Item	Description
Temperature	The two external and the one internal temperature monitors of the LM87. One of the external temperature sensors is part of the processor and the other is mounted at the front of the Orbiter to sense the input air temperature.
Chassis Intrusion	The front door is open

## 10.2. LM87 Limit Setup

These tables control when the LM87 will generate an SMB alert interrupt

Temperature Limits

TBD

Voltage Limits

TBD

Fan Speed Limits

TBD

## 10.3. LM87 Port Assignments

# 11. SMB (I<sup>2</sup>C) BUS ADDRESSING

## 11.1. Local I<sup>2</sup>C bus addressing

This table lists the I<sup>2</sup>C addresses of the devices that are on the Orbiter.

Device	Address
DIMM ID	TBD
LM87	0x2C
Orbiter ID	TBD
Clock Control Chip	0x69

## 11.2. System I<sup>2</sup>C addressing

This table lists the I<sup>2</sup>C addresses of the devices that could be detected via the system I<sup>2</sup>C bus. Not all the boards listed in the table below are necessarily installed in a system. If a board is installed it will have a device ID EEPROM. It may not have status device.

Device	Address
HotDockChassis ID EEPROM (on the LED board)	0xA0
Hub Board device ID EEPROM	0xA2
Hub Status	0x40
Power Supply 1 device ID EEPROM	0xA4
Power Supply 2 device ID EEPROM	0xA6
I/O Slot 1 device ID EEPROM	0xA8
I/O Slot 1 Status	0x48
I/O Slot 2 device ID EEPROM	0xAA

Device	Address
I/O Slot 2 Status	0x4A
I/O Slot 3 device ID EEPROM	0xAC
I/O Slot 3 Status	0x4C
I/O Slot 4 device ID EEPROM	0xAE
I/O Slot 4 Status	0x4E

**12. SMB ALERT INTERRUPT**

If the BIOS detects an SMB alert interrupt from the LM87 or the ALI1535 the BIOS will do the following.

If the interrupt was generated as the result of a fault the BIOS will set board fault LED.  
The BIOS will log the fault in its event log

Question: who (BIOS or resident management program) and under what conditions should the board fault LED be reset?

Question: Does system status data cause any kind of interrupt event?

**13. ID SERIAL EEPROM CONTENTS DESCRIPTION****14. DMI TABLE DATA****15. CLOCK GENERATOR SETUP****16. PCI SLOT ASSIGNMENTS**

Component	REQ	GNT	INT	PCI ID	Notes
PCI Slot for debug	0	0	PIRQ0#	AD16	DEBUG Only
LAN Public	1	1	PIRQ1#	AD20	82559ER
LAN Private	2	2	PIRQ2#	AD21	82559ER
LAN Management	3	3	PIRQ3#	AD22	82559ER
ALI 1535 Main				AD18	
ALI 1535 PMU				AD28	
ALI 1535 IDE				AD27	
ALI 1535				AD31	Not used in this

USB					design
ALI 1535 Audio				AD17	Not used in this design
ALI 1535 Modem				AD19	Not used in this design

## 17. FLASH PROGRAMMING

The Orbiter will support remote BIOS updates.

The embedded programming algorithms support the following Flash parts:

Part Number	Manufacturer
AMD29F160DT120EC	AMP

## 18. HARD DISK STARTUP

It is generally a good idea to sequence the start up of the hard disks to reduce the total startup current. It is imperative that hard drive start up be sequenced for Twenty four board systems that have two drives installed on more than half the cards.

## 19. HUB BOARD STATUS MONITORING

### 20. 485 BUS

The HotDock Chassis has a 485 Bus connected to each Orbiter and to the SMC slot. This is a half duplex 485 type bus.

The Orbiter can communicate through this bus using its COM2 port. The receive side is always enabled. The transmit side is enabled by raising the COM2 RTS.

The bus can either be used as a polled bus with a single computer serving as the master (probably the computer with the MASTER signal high). Or the bus can be used for multi-drop communication. If this approach is used it is up to the application to appropriately detect and recover from collisions.

## 21. GPIO ASSIGNMENTS FOR RLXORB

## 21.1. Outputs

SIGNAL NAME	FUNCTION	GPIO PIN	Default Type	PIN #	Voltage	State After BIOS Init
FAN_HI	0=Fan LOW 1=Fan HIGH	SCLK/PDMA_REQ#/RUN_ENT14, GPIO14	I	E4	3.3v/5v IN 5v OUT	GPO, HIGH
BRD_FAULT_LED	0=LED Off 1=LED On	FANOUT1/RUN_ENT8/GPIO8	0,H	W5	3.3v/5v IN 5v OUT	GPO, (note 1)
BRD_GD_LED	0=LED On 1=LED Off	RUN_ENT0/GPIO0	I	Y3	3.3v/5v IN 5v OUT	GPO, (note 2)
ORB_LED	0=LED Off 1=LED On	FANIN2/GPIO19	I	Y5	3.3v/5v IN 5v OUT	GPO, (note 3)
FLASHWE#	0=Enable Write to Flash 1=Flash Write Protected	FANOUT2/RUN_ENT8/GPIO8	0,H	V5	3.3v/5v IN 5v OUT	GPO, HIGH
LOCAL_I2C_SEL	0=System I2C selected 1=Local I2C selected	ACGP_UP#/RUN_ENT11/GPIO11	IPH	U3	3.3v/5v IN 5v OUT	GPO, HIGH

Note 1 - The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW when POST exits if an error was not detected. The BIOS causes this output to flash the POST result if an error was detected.

Note 2 - The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW to when POST exists if an error was not detected.

Note 3 - The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW when POST exits if an error was not detected. The BIOS causes this output to flash the POST result if an error was detected.

## Command Bus

The BIOS sets these ports to Outputs. The signals are buffered and disabled on every board unless the master signal is active for the slot the board is installed in.

SIGNAL NAME	FUNCTION	GPIO PIN	Default Type	PIN #	Voltage	Pin type and state after BIOS init
MBADD0_OUT	Management Bus address 0	HDSEL#/RUN_ENT19/EGPIO3	O	M19		GPO, LOW

MBADD1_OUT	Management Bus address 1	ACGP_DOWN#/RUN_ENT12/ GPIO12	IPH	R5	3.3v/5v IN 5v OUT	GPO, LOW
MBADD2_OUT	Management Bus address 2	ACGP_MUTE#/RUN_ENT13/ GPIO13	IPH	U2	3.3v/5v IN 5v OUT	GPO, LOW
MBADD3_OUT	Management Bus address 3	DENSEL/EGPIO14	O	J19	3.3v/5v IN 5v OUT	GPO, LOW
MBADD4_OUT	Management Bus address 4	ACGAME [6], GPIO18	IPH	Y1	3.3v/5v IN 5v OUT	GPO, LOW
MBADD5_OUT	Management Bus address 5	LFRAME#/RUN_ENT5, GPIO5	O	N20	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD0_OUT	Management Bus command line 0	LDRQ#/RUN_ENT4, GPIO4	I	P17	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD1_OUT	Management Bus command line 1	ACGAME [2], GPIO16	I	V3	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD2_OUT	Management Bus command line 2	ACGAME [3], GPIO17	I	W1	3.3v/5v IN 5v OUT	GPO, LOW
MBSTROBE_OUT #	Management Bus strobe	MOT1#/GPIO10	O/HI	K18	3.3v/5v IN 5v OUT	GPO, HIGH

## 21.2. Inputs

SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
MASTER	0=This board is not master 1=This board is master	WPROT#/EGPIO11	IPH	M16	3.3v/5v IN 5v OUT	GPI
PASSWRDRST#	0=Password Reset Button Pushed 1=Normal	RUN_ENT1/GPIO1	I	V4	3.3v/5v IN 5v OUT	GPI, Interrupt
SLOTID0	Board ID 0	FD_DIR#/EGPIO4	O	L16	3.3v/5v IN 5v OUT	GPI
SLOTID1	Board ID 1	STEP#/EGPIO5	O	L17	3.3v/5v IN 5v OUT	GPI
SLOTID2	Board ID 2	WGATE#/EGPIO1	O	L19	3.3v/5v IN 5v OUT	GPI
SLOTID3	Board ID 3	DRV0#/EGPIO7	O	K19	3.3v/5v IN 5v OUT	GPI



SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
SLOTID4	Board ID 4	DRV1#/EGPIO8	O	K20	3.3v/5v IN 5v OUT	GPI
SLOTID5	Board ID 5	MOT0#/EGPIO9	O	K17	3.3v/5v IN 5v OUT	GPI
PSACOK1#	0=Power Supply 0 AC OK 1=Power Supply 0 AC Not OK	RDATA#/EGPIO0	I	M18	3.3v/5v IN 5v OUT	GPI
PSACOK2#	0=Power Supply 1 AC OK 1=Power Supply 1 AC Not OK	PCMDATA/RUN_ENT10, GPIO10	IPH	T3	3.3v/5v IN 5v OUT	GPI
PSFAIL1	0=Normal 1=Power Supply 0 Failure	GP124	I	M17	3.3v/5v IN	GPI
PSFAIL2	0=Normal 1=Power Supply 1 Failure	GP125	I	E9	3.3v/5v IN	GPI
PSPRESENT1#	0=Power Supply 0 Present 1=Power Supply 0 Not Present	OVCRO#/GPIO20	IPH	T5	3.3v/5v IN 5v OUT	GPI
PSPRESENT2#	0=Power Supply 1 Present 1=Power Supply 1 Not Present	OVCRI#/GPIO21	IPH	T6	3.3v/5v IN 5v OUT	GPI
PSPWROK1	0=Power Supply 0 Power OK 1=Power Supply 0 Power Not OK	OVCRI2#/GPIO22	IPH	U5	3.3v/5v IN 5v OUT	GPI
PSPWROK2	0=Power Supply 1 Power OK 1=Power Supply 1 Power Not OK	OVCRI3#/GPIO23	IPH	U6	3.3v/5v IN 5v OUT	GPI
PSPRFAIL1	0=No power supply fail predicted 1=Power supply fail predicted	DSKCHG#/EGPIO6	I	M20	3.3v/5v IN 5v OUT	GPI
PSPRFAIL2	0=No power supply fail predicted 1=Power supply fail predicted	LRCLK/PDMA_GNT#/RUN_E NT15, GPIO15	I	E5	3.3v/5v IN 5v OUT	GPI
FLASHRDY#	0=Flash Busy 1=Flash Ready	ACGAME[7], GPIO19	I	Y2	3.3v/5v IN 5v OUT	GPI
IDECDP	Cable detect for 66mhz UDMA primary 80pin	AGP_BUSY#/GPIO26/CBLID_P	I	D11	3.3v/5v IN	CBLID_P
IDECDS	Cable detect for 66mhz UDMA secondary 80 pin	AGP_STP#/GPIO33/CBLID_S	I	E11	3.3v/5v IN	CBLID_S

SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
BRD_FAULT#	0=Board fault exists in system 1=No board faults in system	TRK0#/EGPIO12	IPH	L20	3.3v/5v IN 5v OUT	GPI
SYS_FAULT#	0=System fault exists 1=No board faults	INDEX#/EGPIO13	IPH	I20	3.3v/5v IN 5v OUT	GPI
CMDBUS_EVNT	0=no command bus event 1= command bus event present	RUNENT2/GPIO2	I	W4	3.3v/5v IN 5v OUT	GPI, Interrupt Output of command bus decode
TST_BRD_PRES_IN#	0=Orbiter responded to command bus present query 1=no response to command bus query	RUNENT3/GPIO3	I	Y4	3.3v/5v IN 5v OUT	GPI This signal is read by MASTER computer only

### 21.3. Spares

GPIO PIN	Def Type	PIN #	Voltage	Notes
WGATE#/RUN_ENT18/EGPIO2	O	L18	3.3v/5v IN 5v OUT	
SLOWDOWN/GPIO21 (not available when over1# used for GPIO21)	O	D9	3.3v/5v IN 3.3V OUT	GPIO21 is being used so this isn't really a spare

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**EXHIBIT B**

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**Anigma**  
Inc.

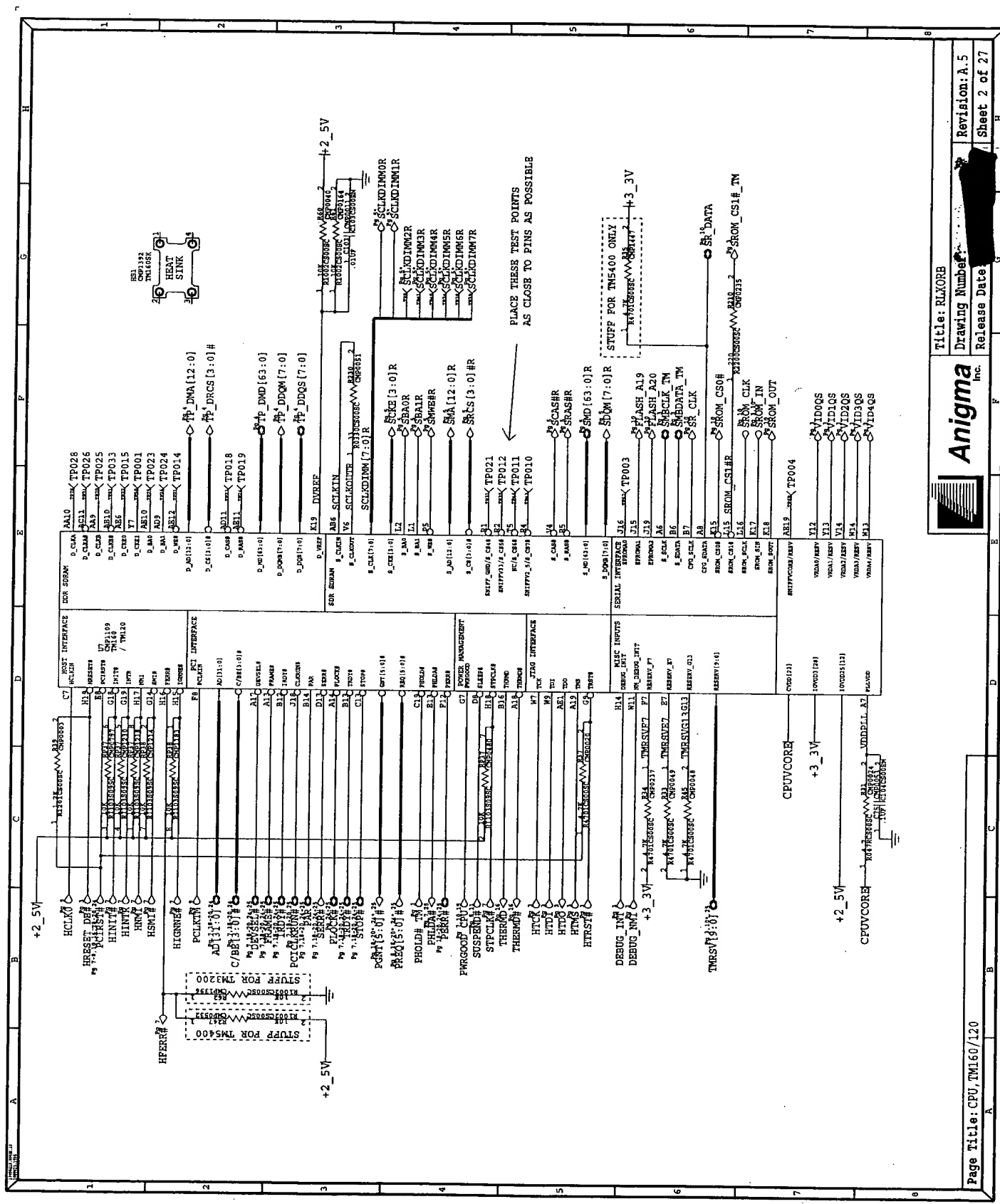
Title: RLXORE

Drawing Number:

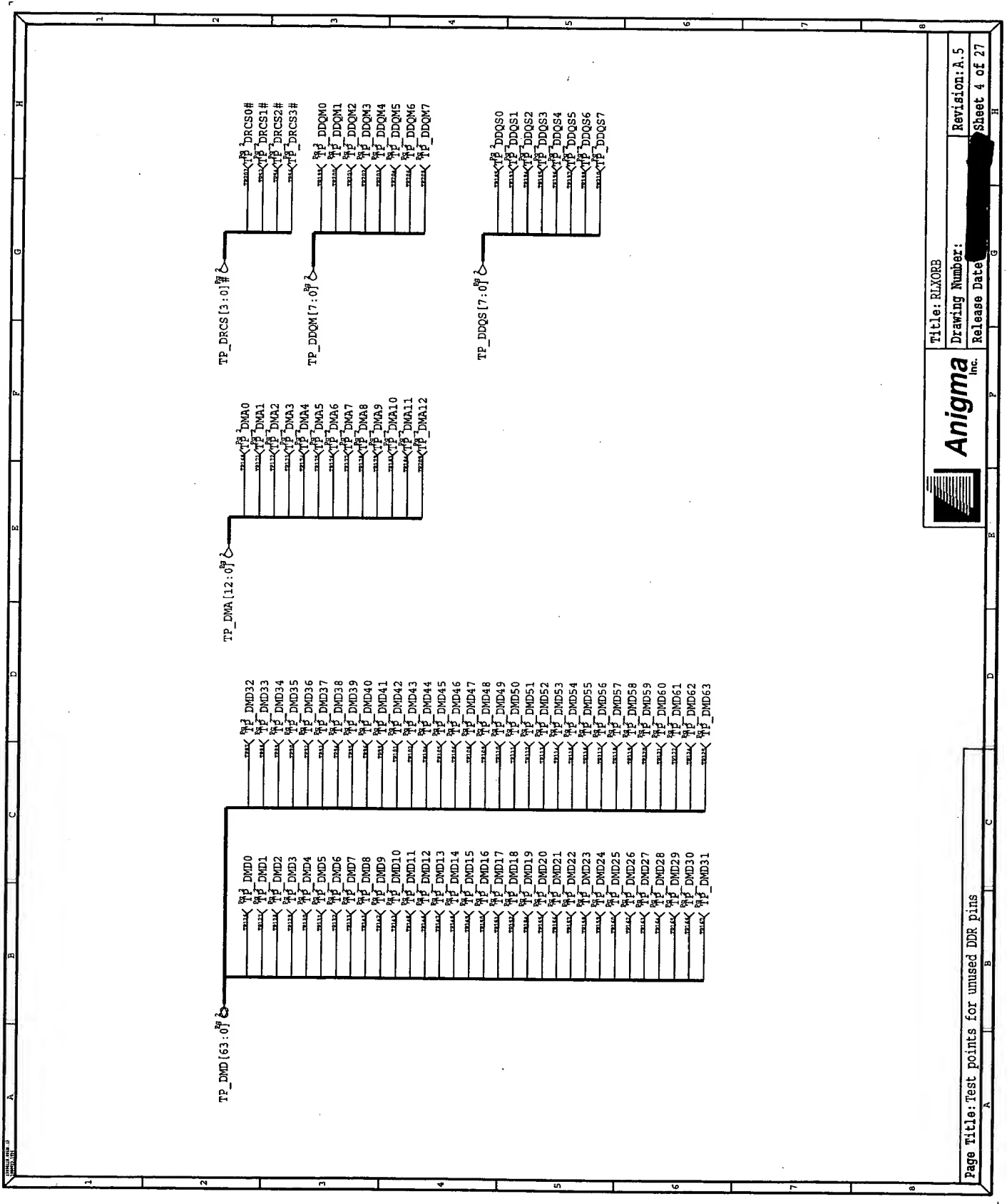
Release Date


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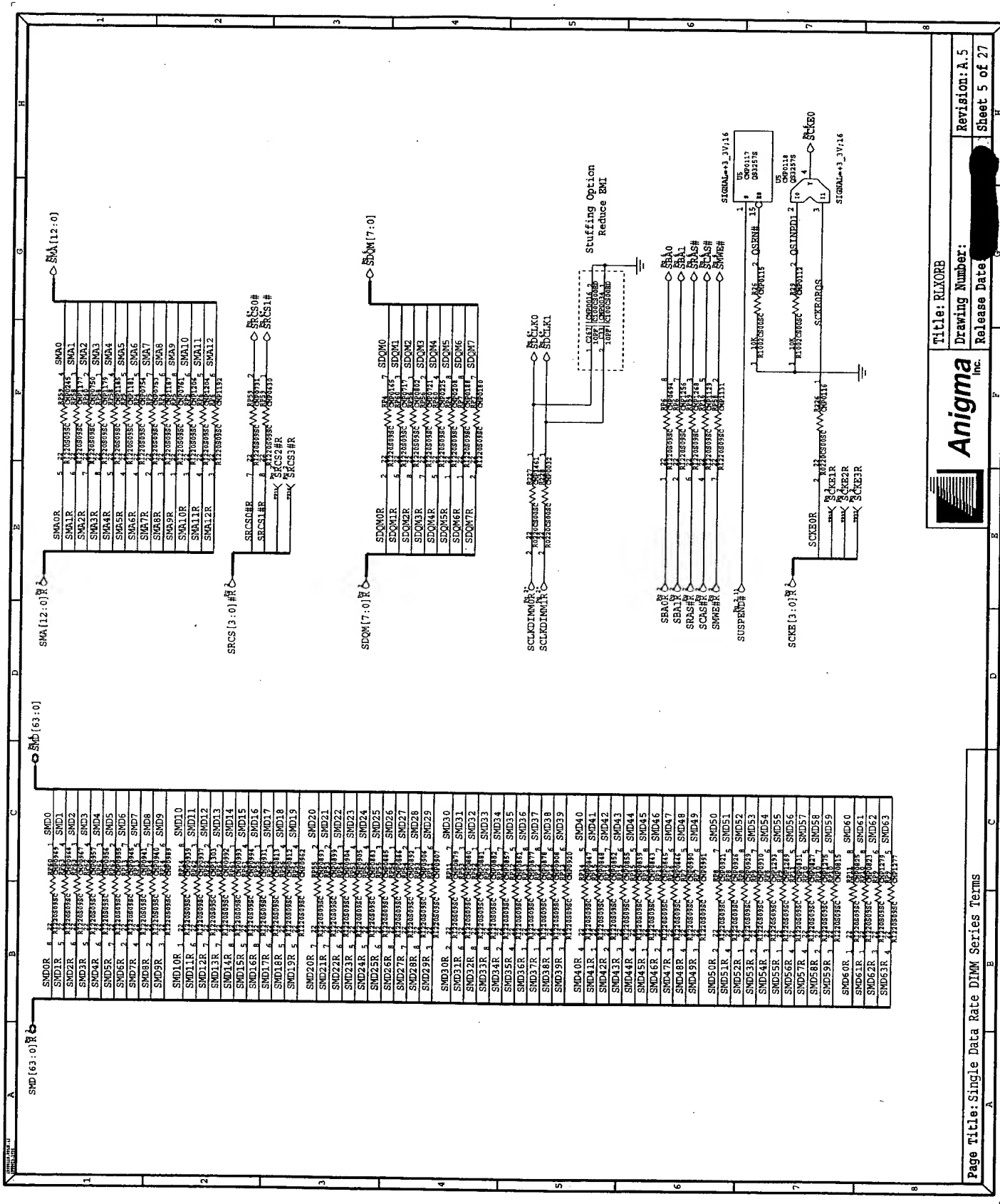
**Anigma**  
Inc.

Title: RLXORB

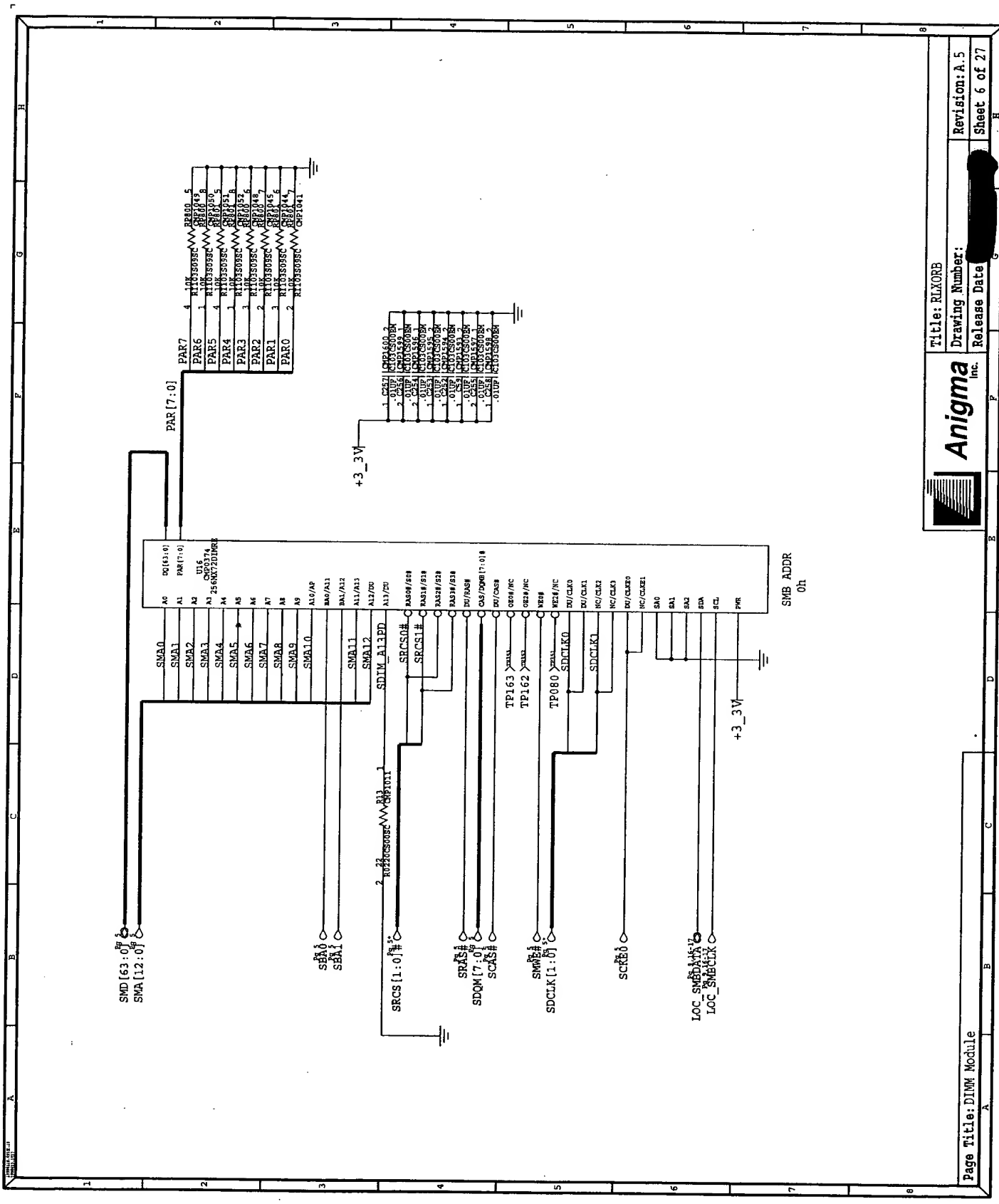
Drawing Number: [REDACTED]

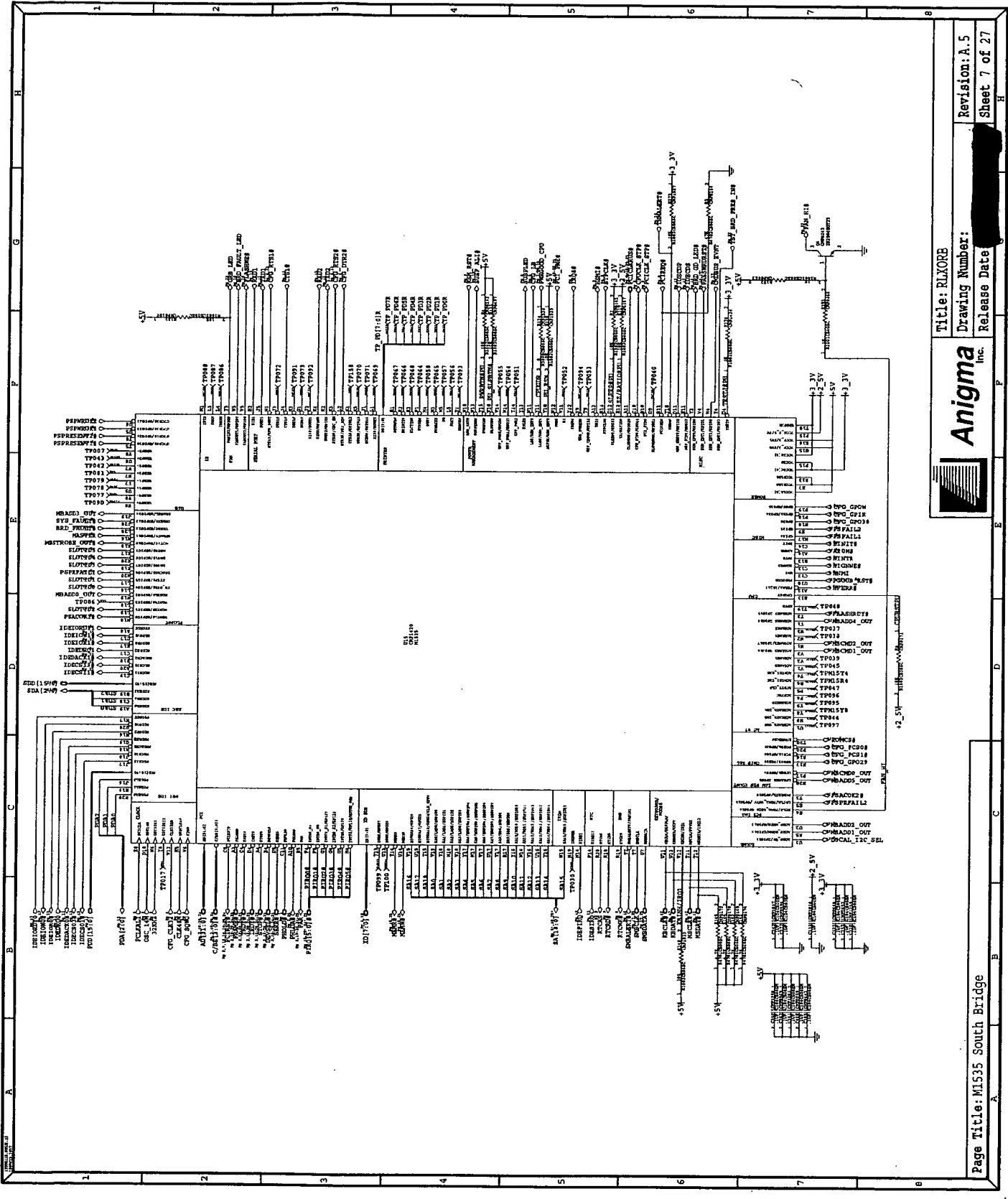
Release Date: [REDACTED]

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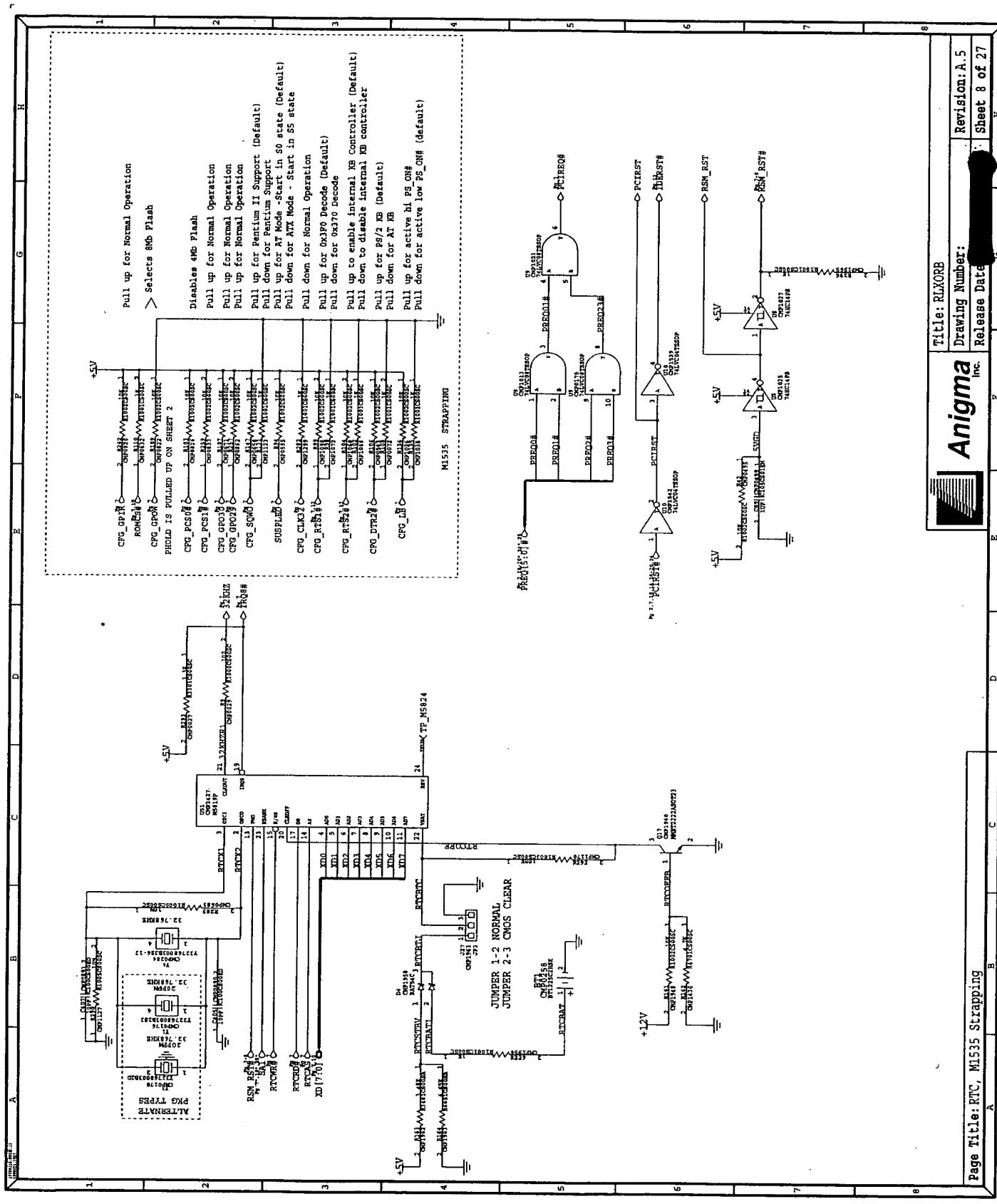




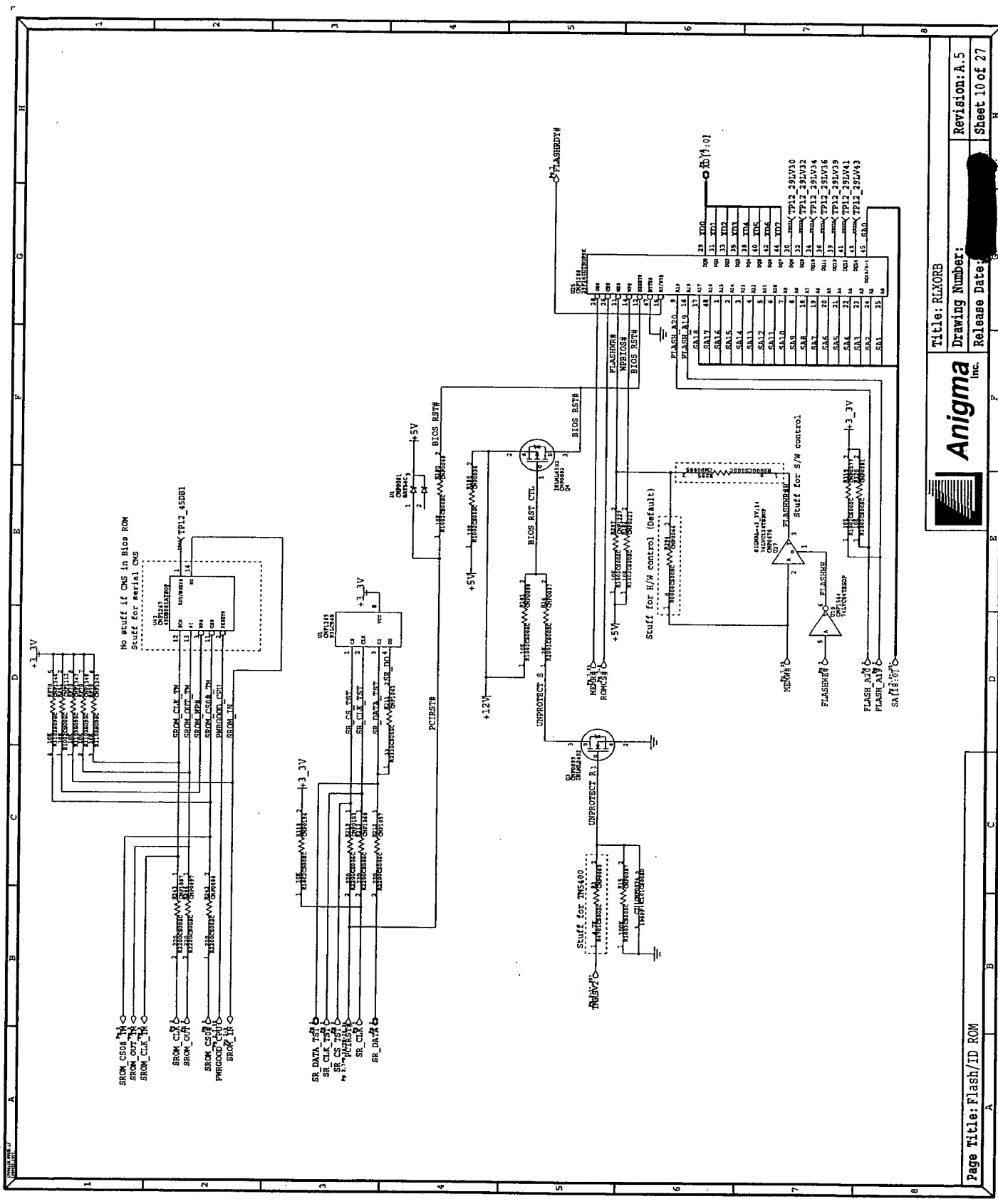


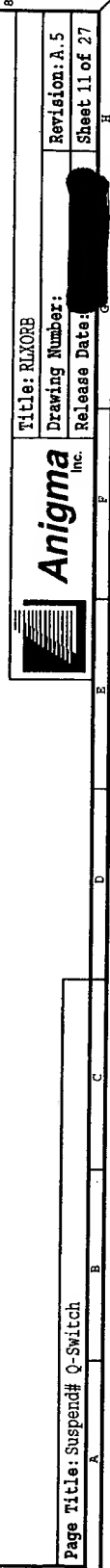
Title: RIXORE  
Drawing Number: [redacted]  
Release Date: [redacted]  
Revision: A.5  
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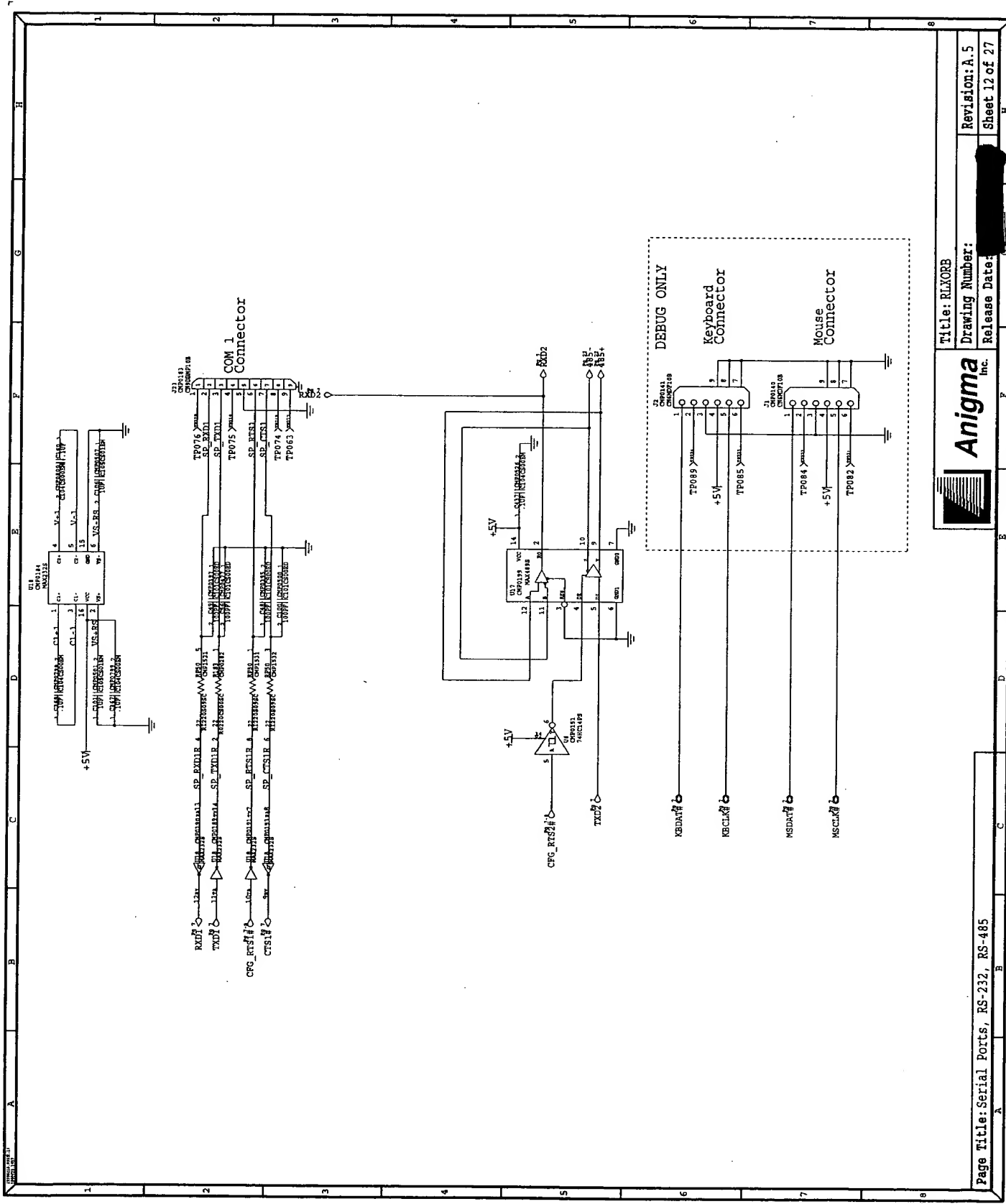






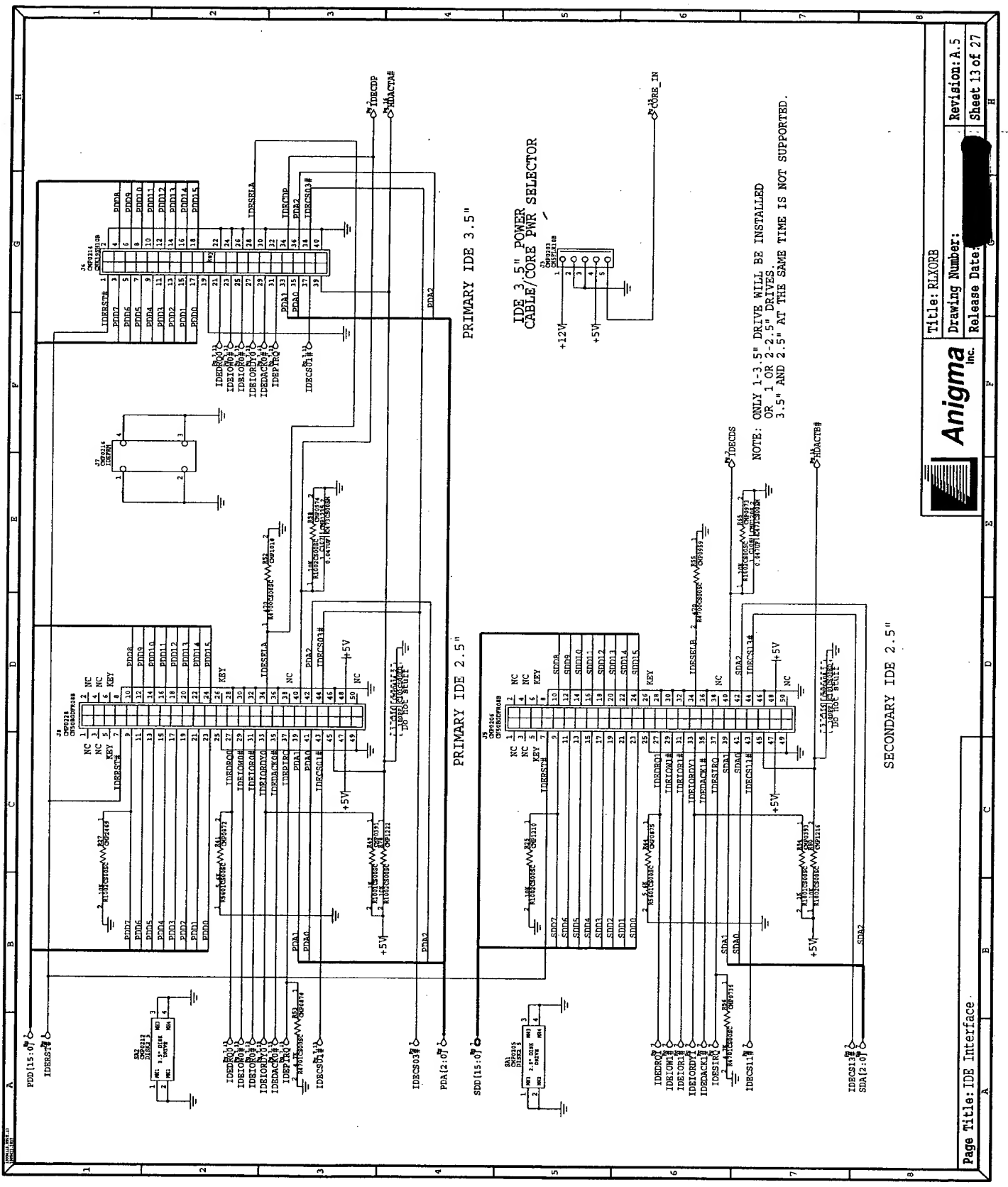






**Anigma Inc.**

Title: RLXORB  
 Drawing Number:  
 Release Date:



**Anigma Inc.**

Title: RLXORB

Drawing Number:

Release Date:

Revision: A.5

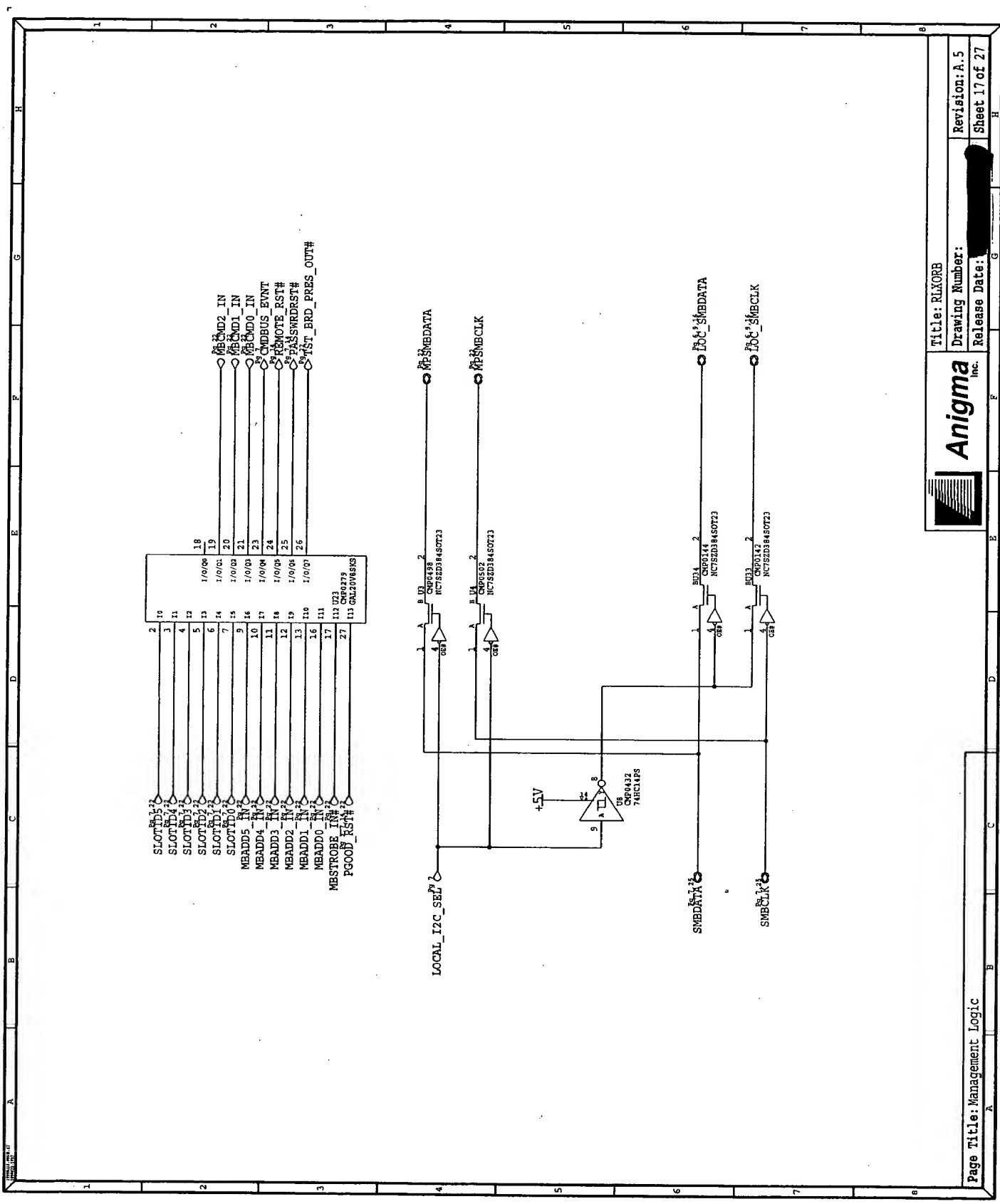
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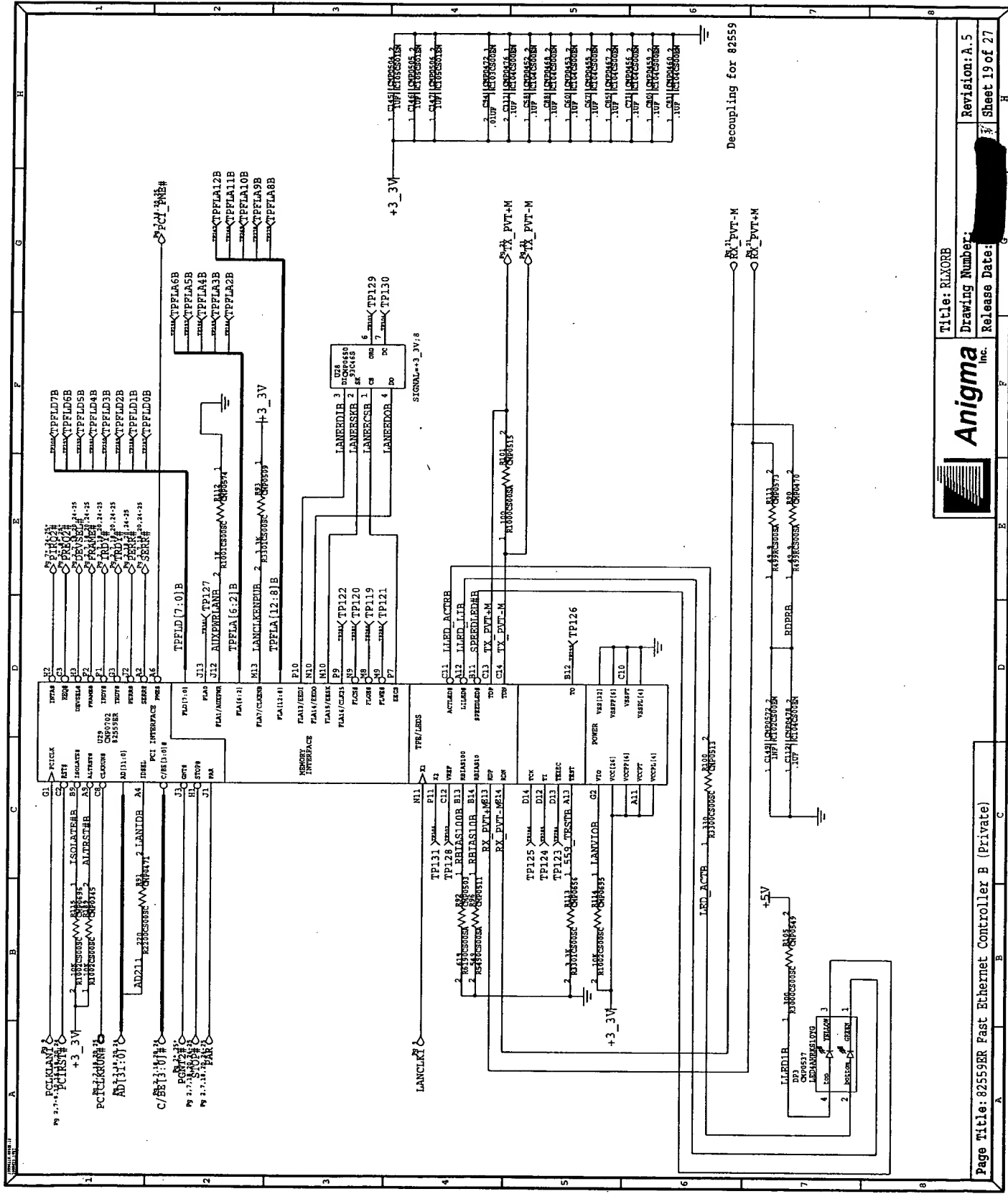










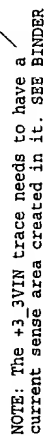




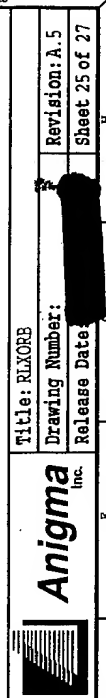




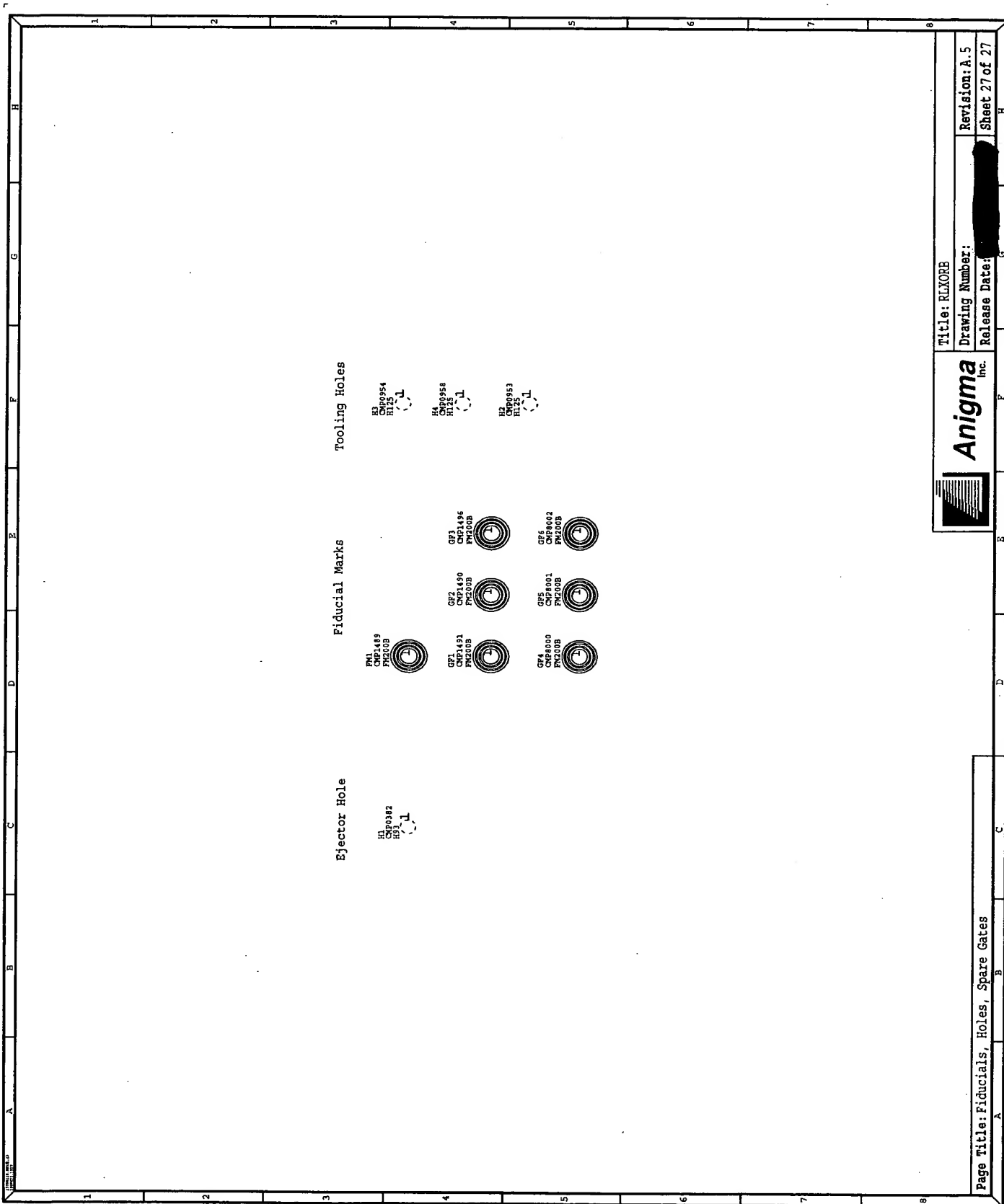




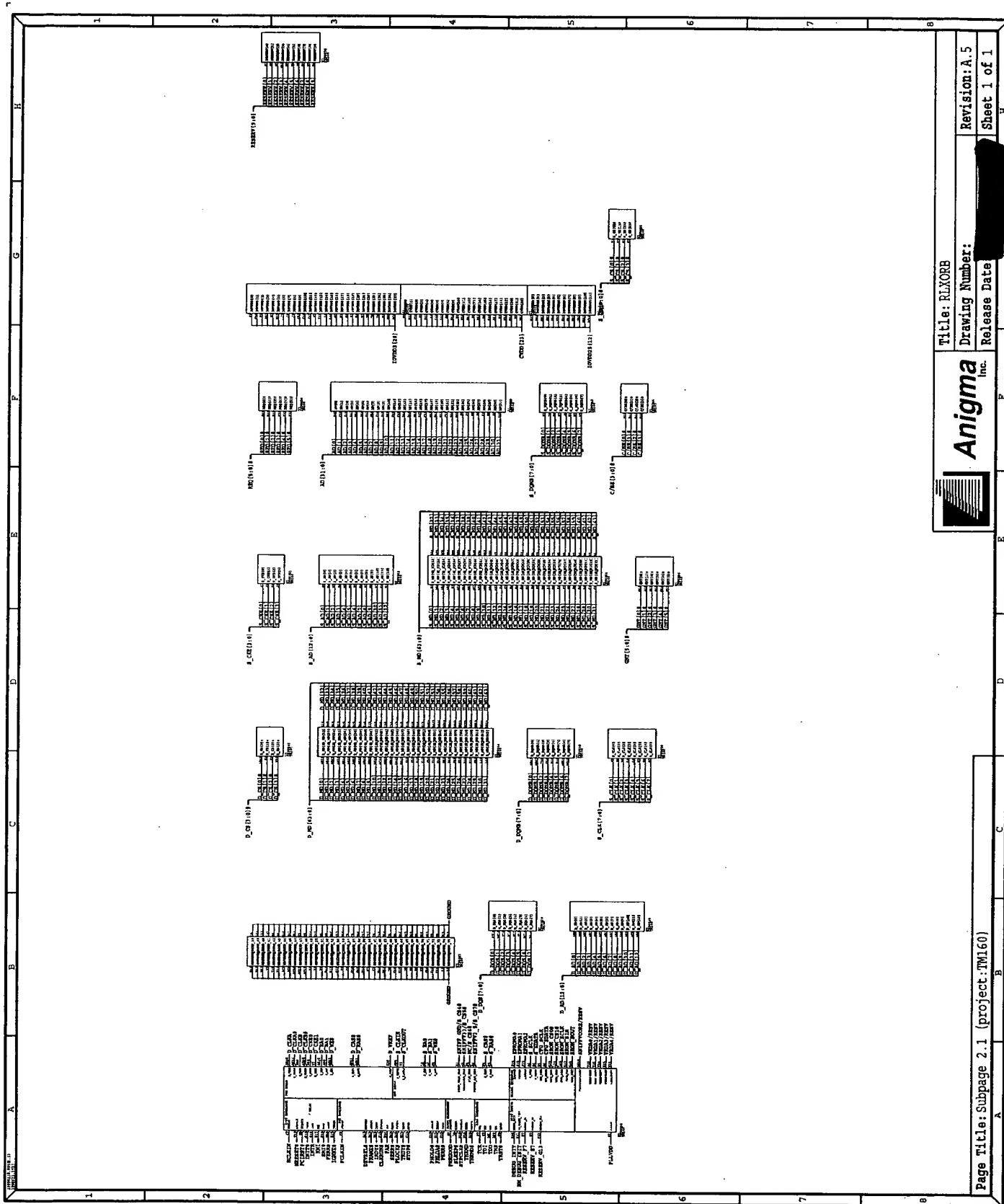


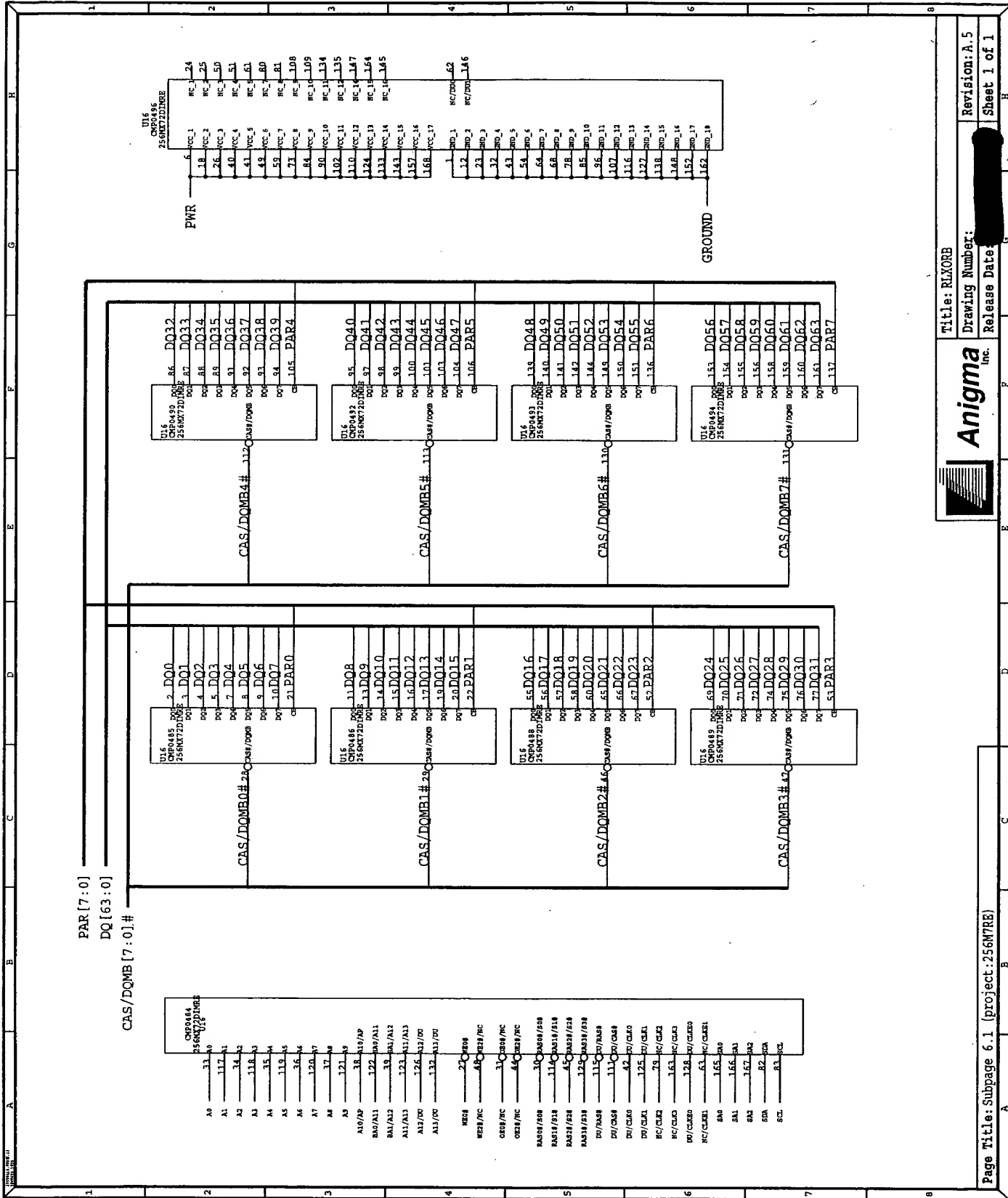






Page Title: Fiducials, Holes, Spare Gates		Title: RLXORB	
Revision: A.5		Drawing Number:	
Sheet 27 of 27		Release Date:	





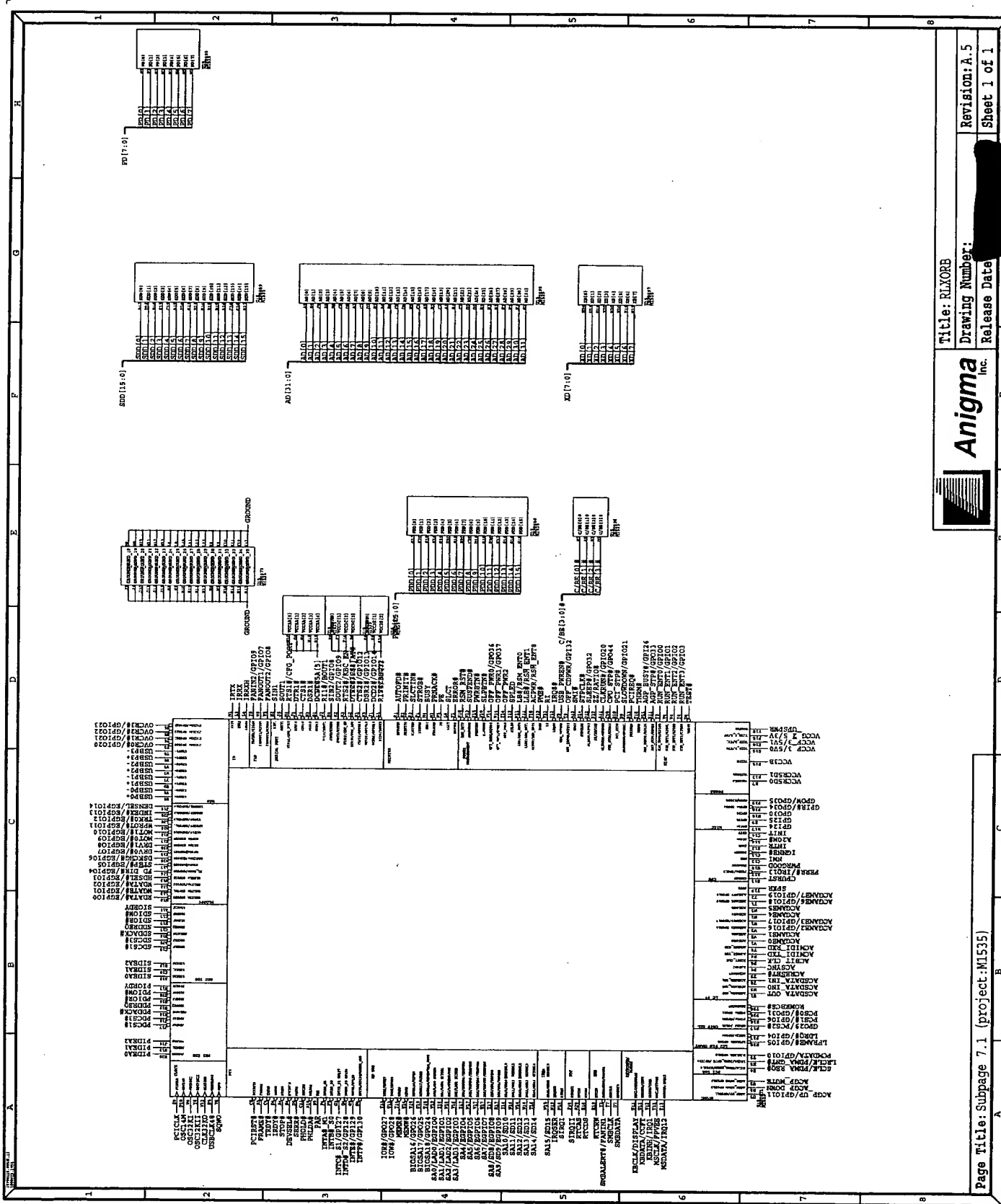
**Anigma**  
Inc.

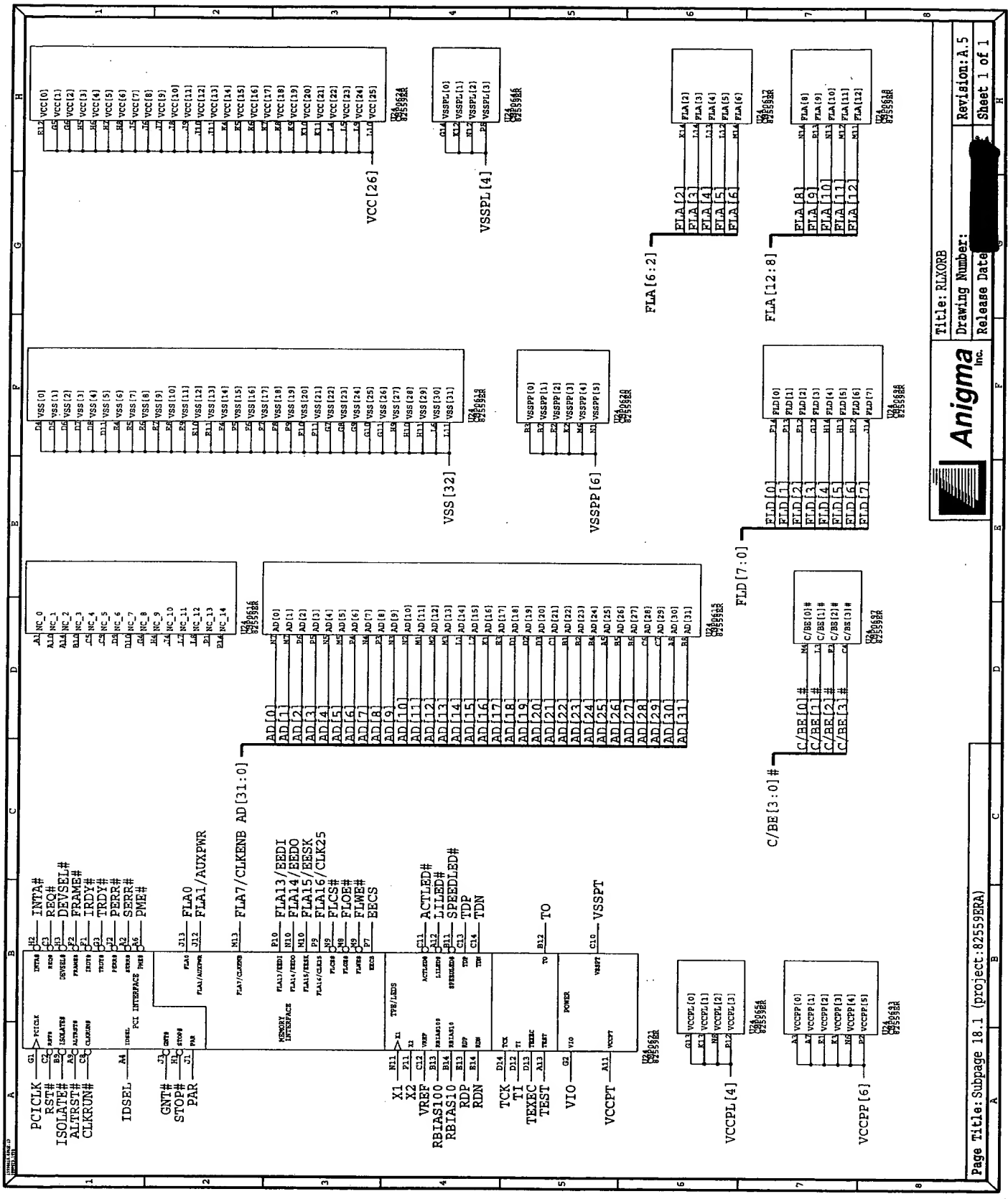
Title: RLXORB  
Drawing Number: [REDACTED]  
Release Date: [REDACTED]

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Page Title: Subpage 6.1 (project: 256M7RE)









Title: RLXORB

Drawing Number: [REDACTED]

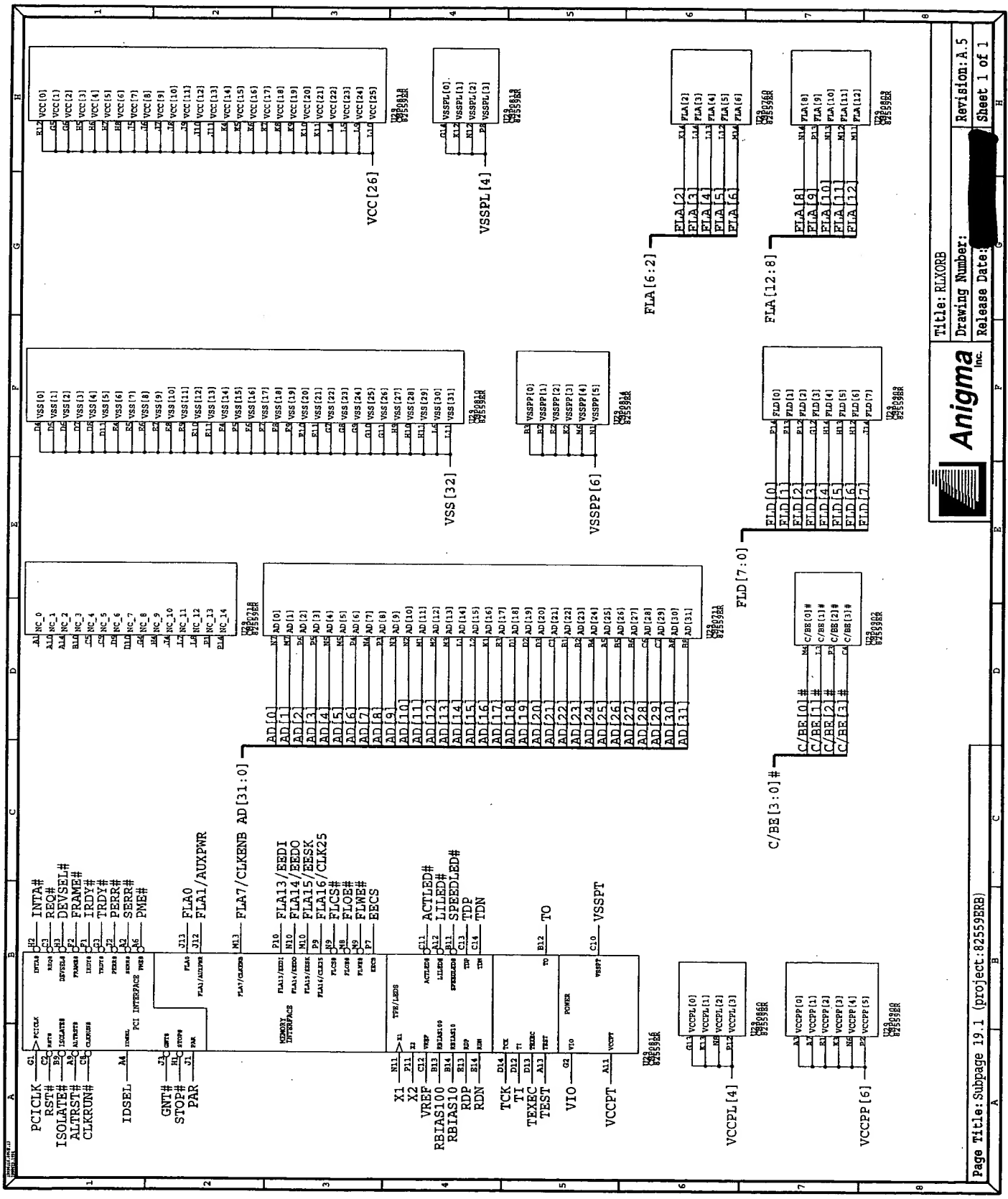
Release Date: [REDACTED]


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Page Title: Subpage 18.1 (project: 82559BRA)

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**Anigma**  
Inc.

Title: RLXORB  
Drawing Number: XXXXXXXXXX  
Release Date: XXXXXXXXXX

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**Anigma**  
Inc.

Title: RLXORB  
Drawing Number:  
Release Date:

Revision: A.5  
 Sheet 1 of 1

ATTORNEY DOCKET NO.  
067856.0213

PATENT APPLICATION  
09/848,816

**EXHIBIT C**

Page# Page Title

- 1 Index
- 2 CPU, TM160/120
- 3 TM debug Port, Decoupling, ect....
- 4 Test points for unused DDR pins
- 5 Single Data Rate DIMM Series Terms
- 6 DIMM Module
- 7 M1535 South Bridge
- 8 RTC, M1535 Strapping
- 9 Clock Generator
- 10 Flash/ID ROM
- 11 Suspend# Q-Switch
- 12 Serial Ports, RS-232, RS-485
- 13 IDE Interface
- 14 Voltage Monitoring / Reset control
- 15 CPU Core Regulator
- 16 System Monitor, Board ID
- 17 Management Logic
- 18 82559ER Fast Ethernet Controller A (Public)
- 19 82559ER Fast Ethernet Controller B (Private)
- 20 82559ER Fast Ethernet Controller C (Management)
- 21 Lan Magnetics
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- 25 Pullup/Pulldown Resistors
- 26 Decoupling Capacitors
- 27 Fiducials, Holes, Spare Gates

Released Rev. A.6 (000628.1650)



**Anigma**  
Inc.

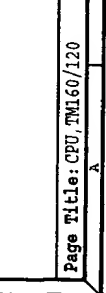
Title: RLXORB

Drawing Number:

Release Date:

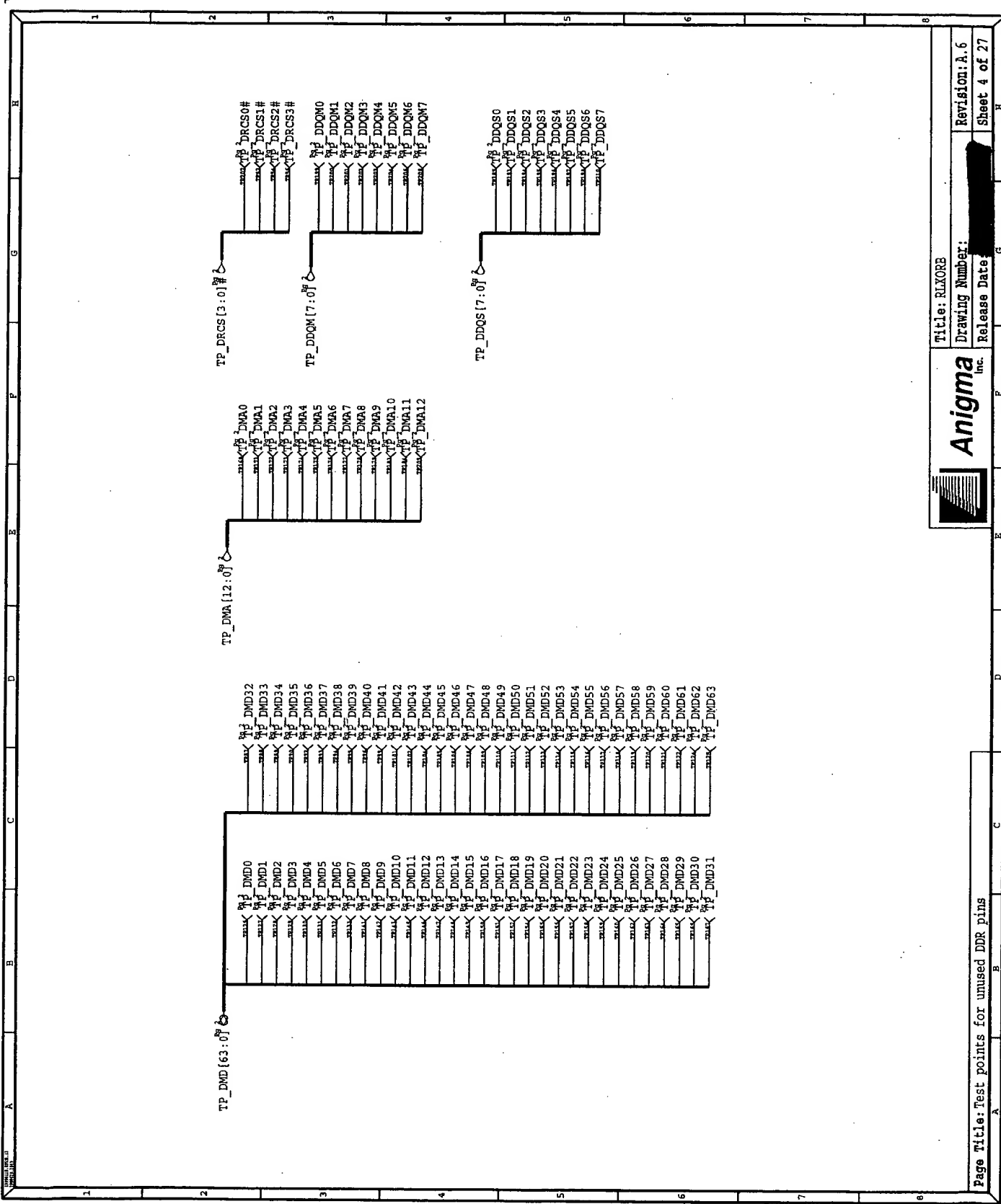
Revision: A.6


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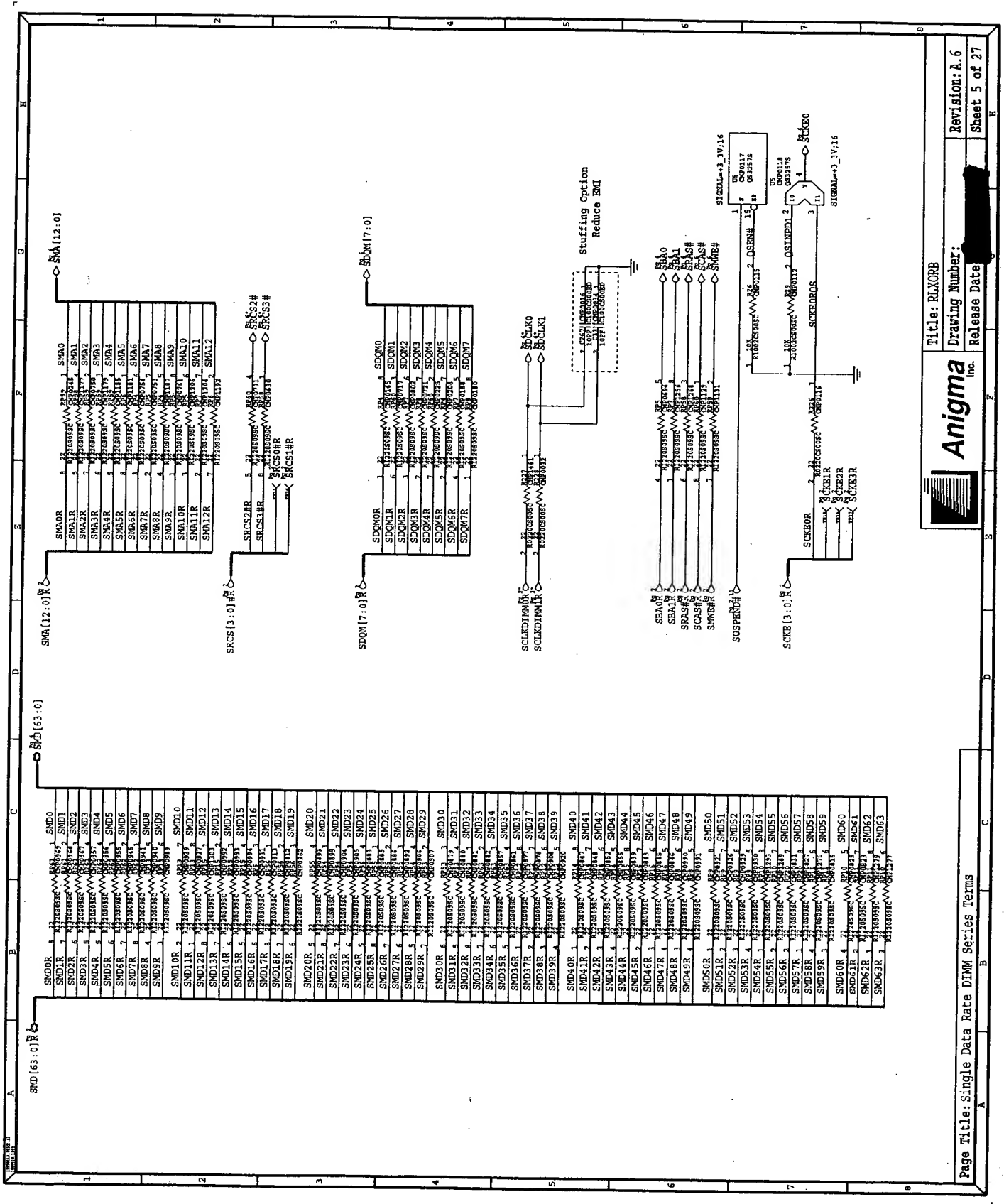
**Anigma**  
Inc.

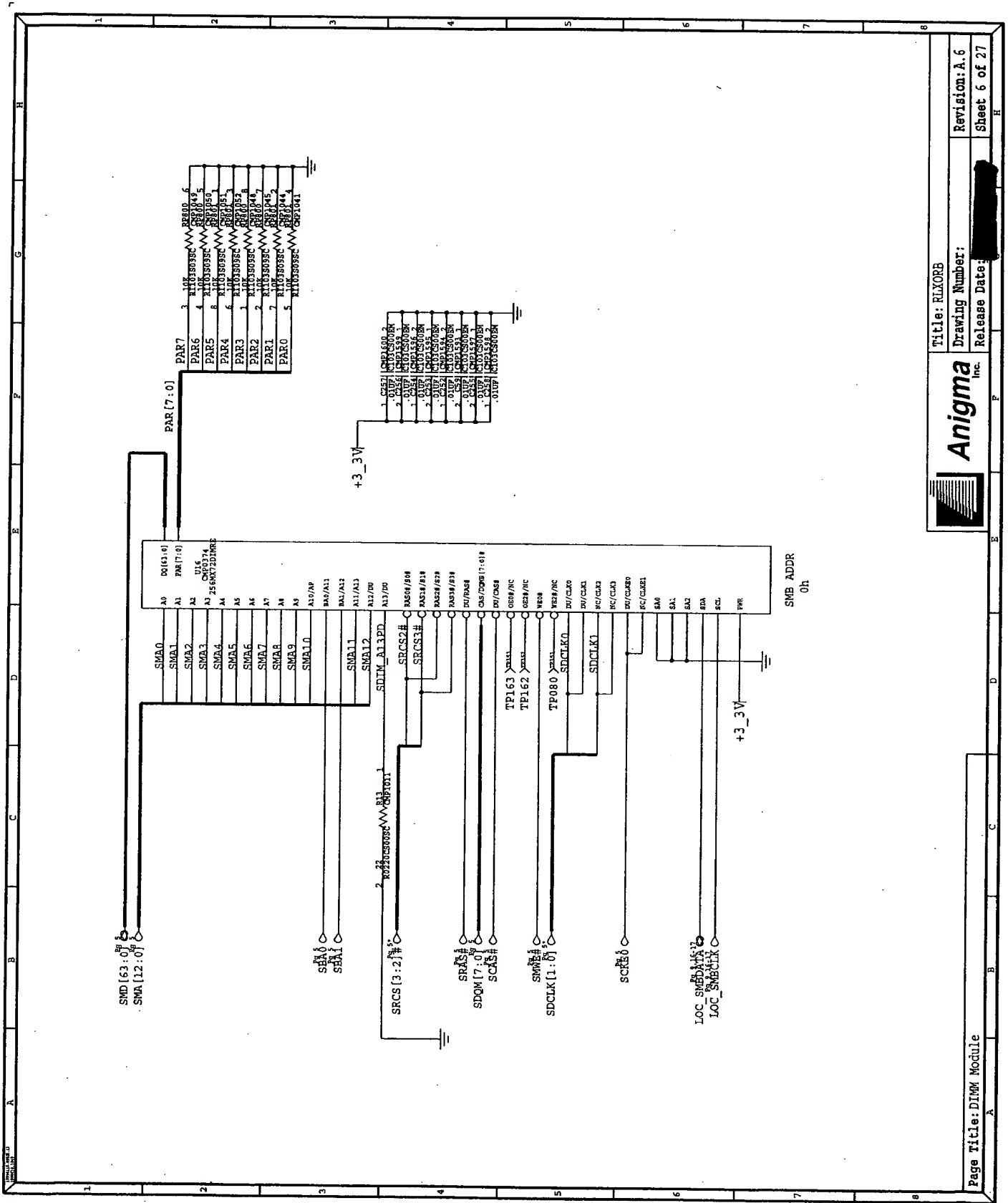
Title: RLX08B


Drawing Number: [REDACTED]

Release Date: [REDACTED]

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**Anigma**  
Inc.

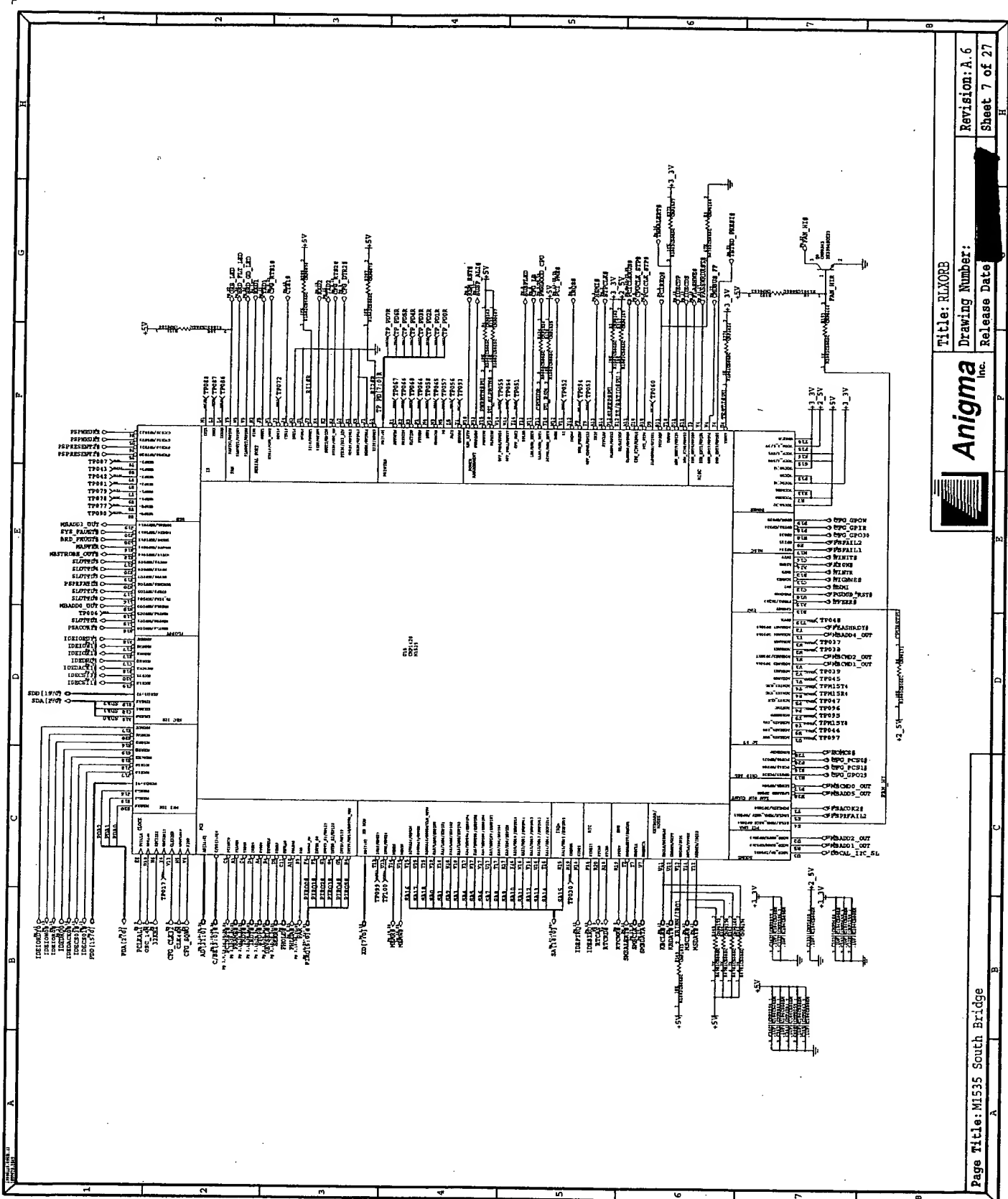
Title: RLXORB

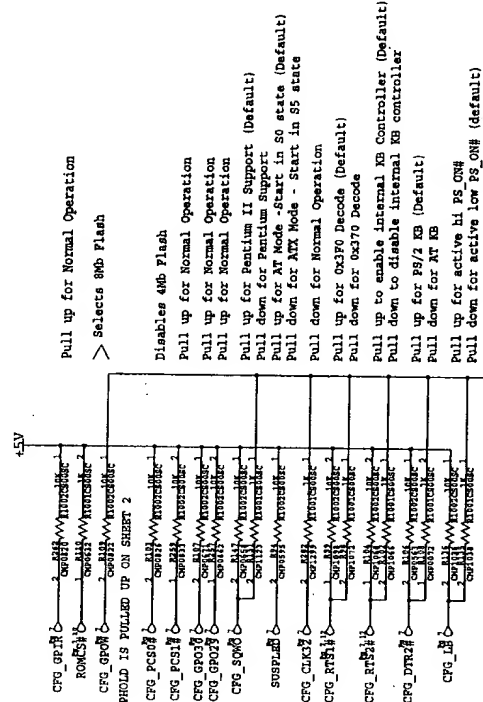
Drawing Number:

Release Date:

Revision: A.6

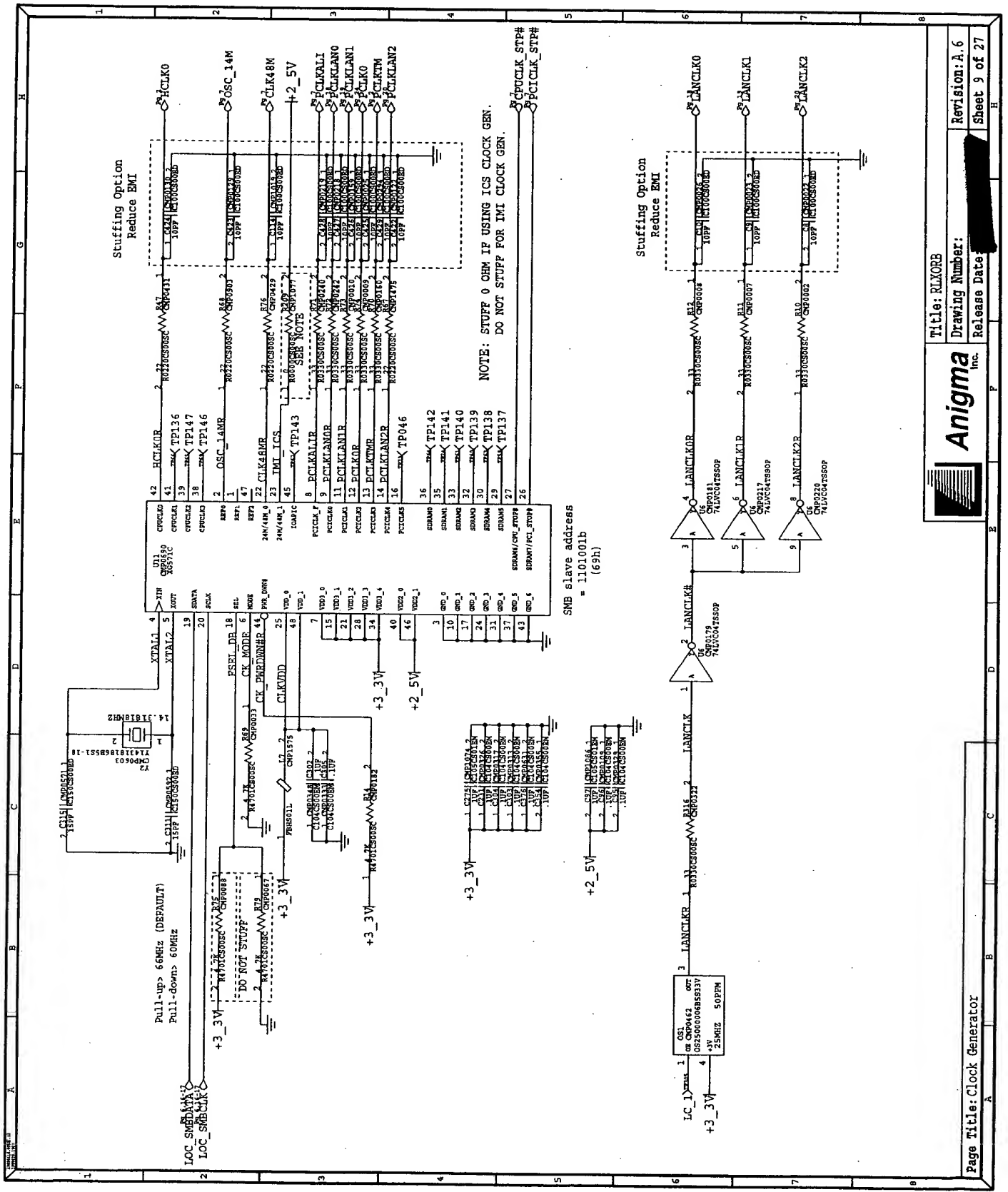
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Inc.

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Page Title: Clock Generator

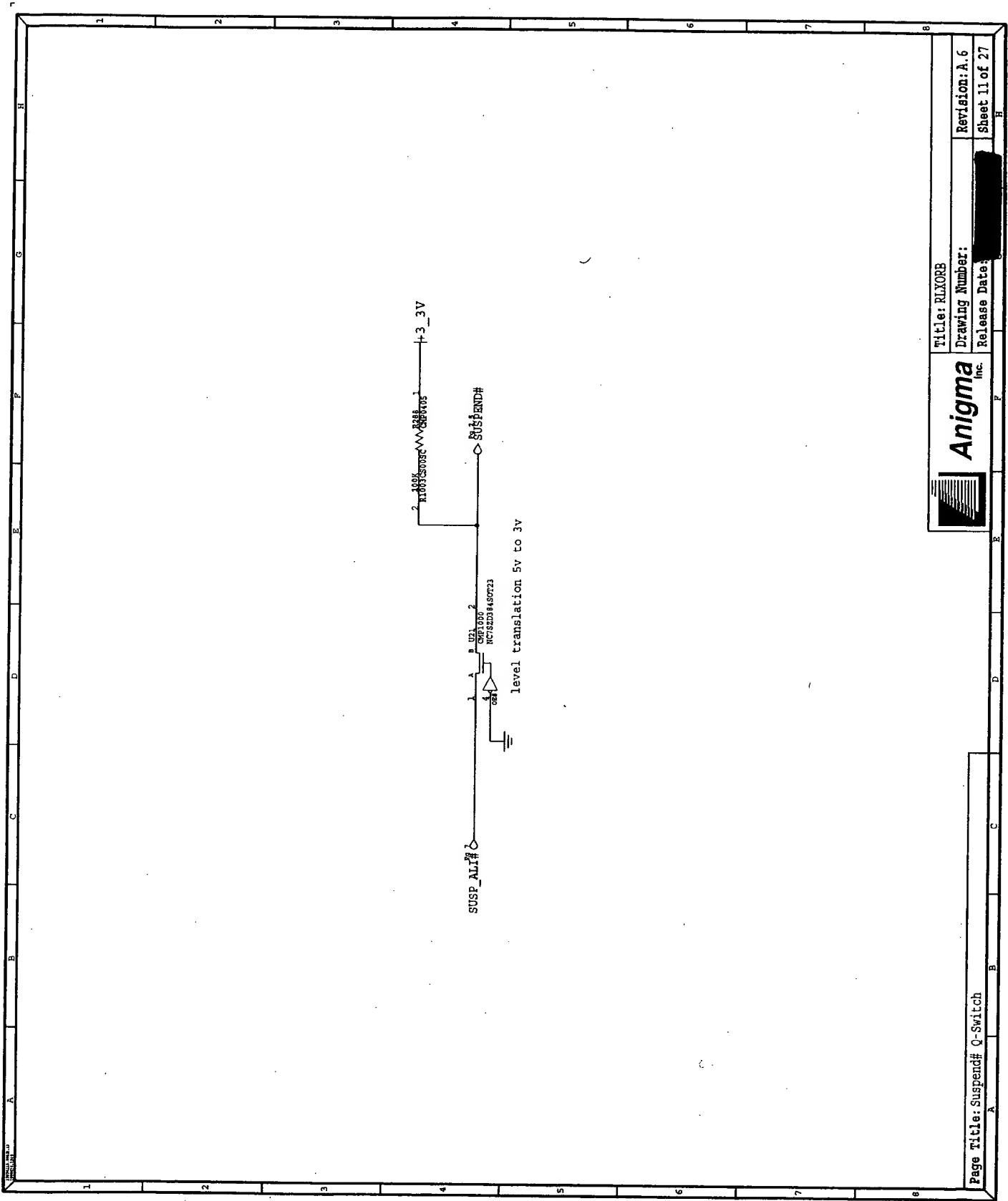
Title: RLXORB

Drawing Number:

Revision: A.6

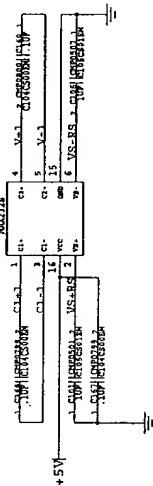
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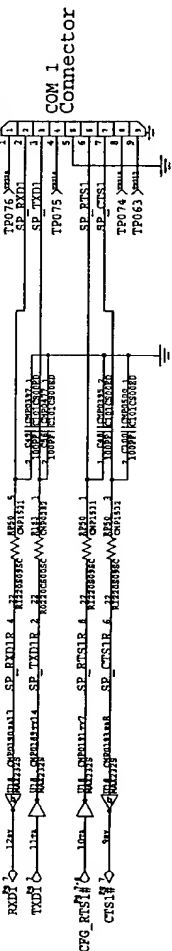




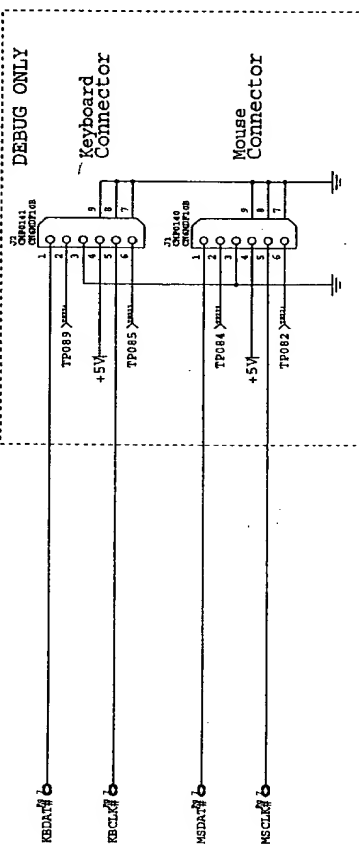
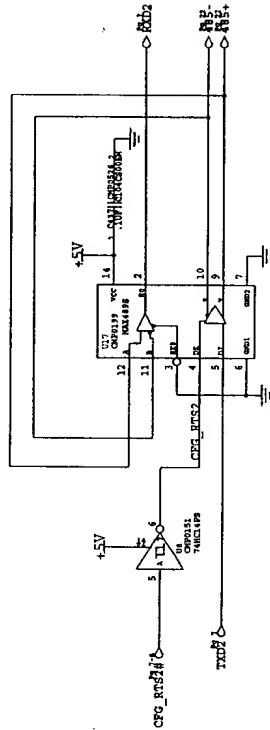
U14  
MAX232



231  
CONVERTER



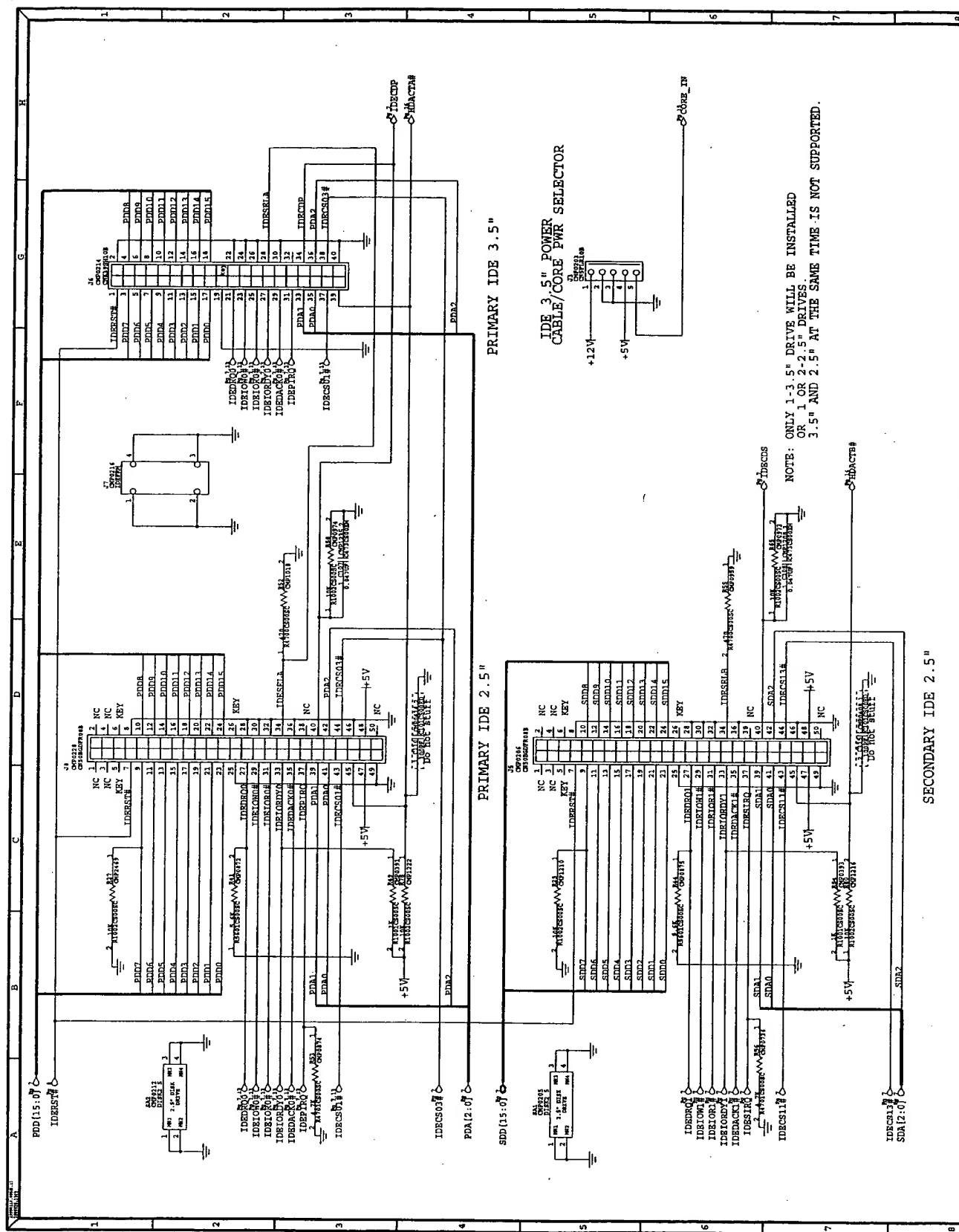
COM 1  
Connector



Title: RLXORB  
Drawing Number:  
Release Date:

Anigma  
Inc.

Revision: A.6  
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ONLY 1-3.5" DRIVE WILL BE INSTALLED  
OR 1 OR 2-2.5" DRIVES.  
3.5" AND 2.5" AT THE SAME TIME IS NOT SUPPORTED.

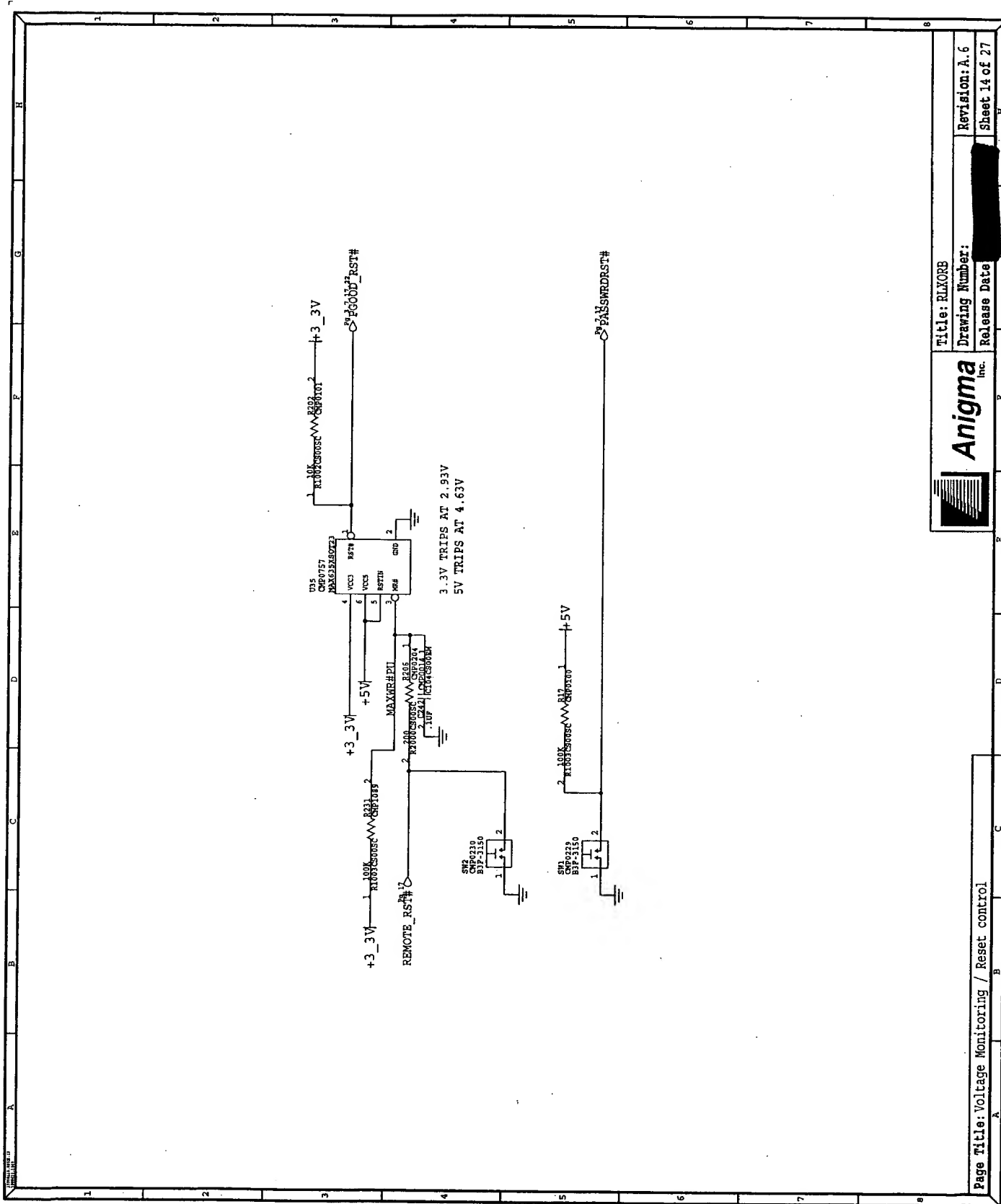
Revision: A.6  
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Title: RLXORB
Drawing Number:
Release Date



**Anigma**<sup>INC.</sup>

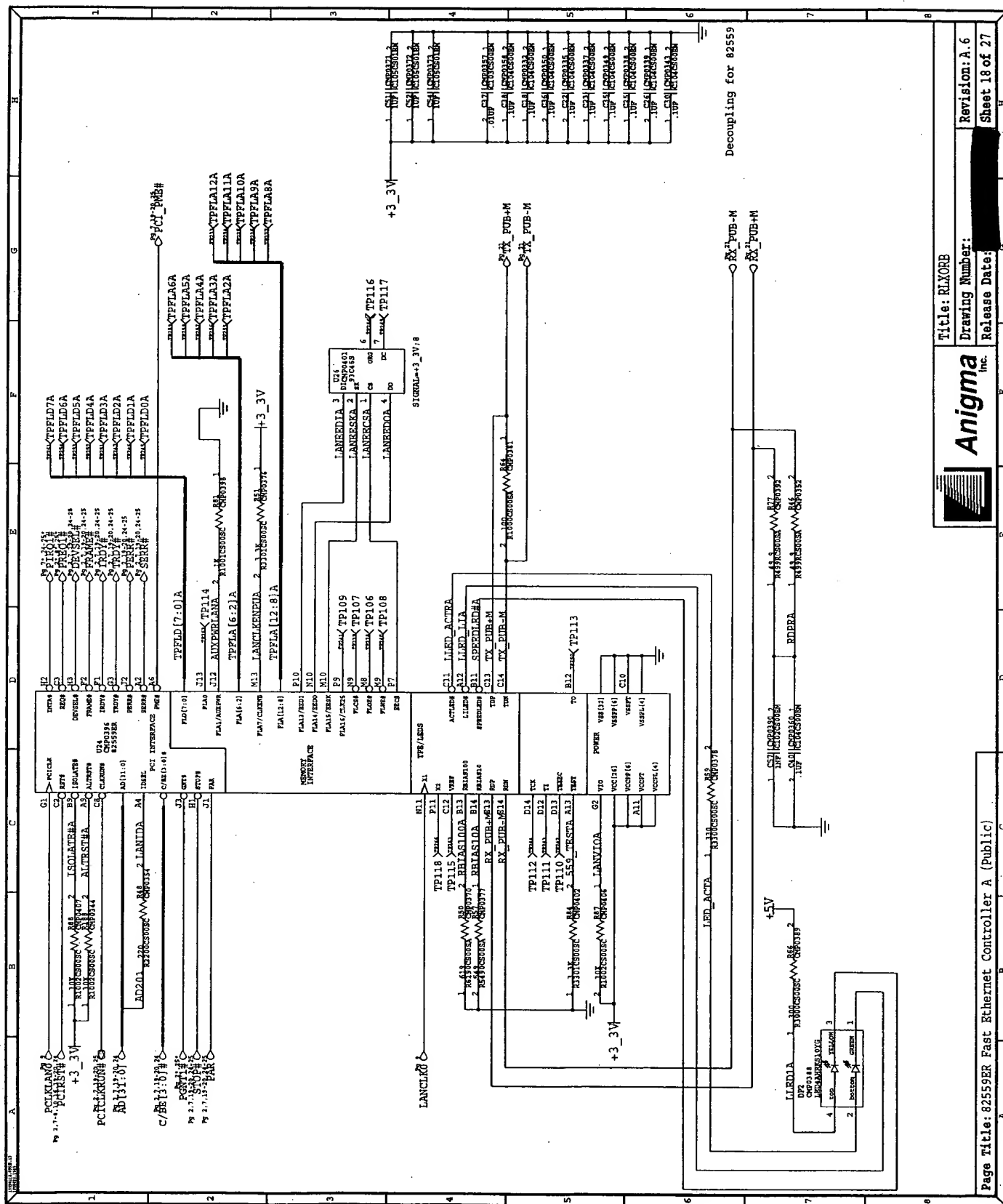
Page Title: IDE Interface

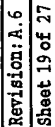










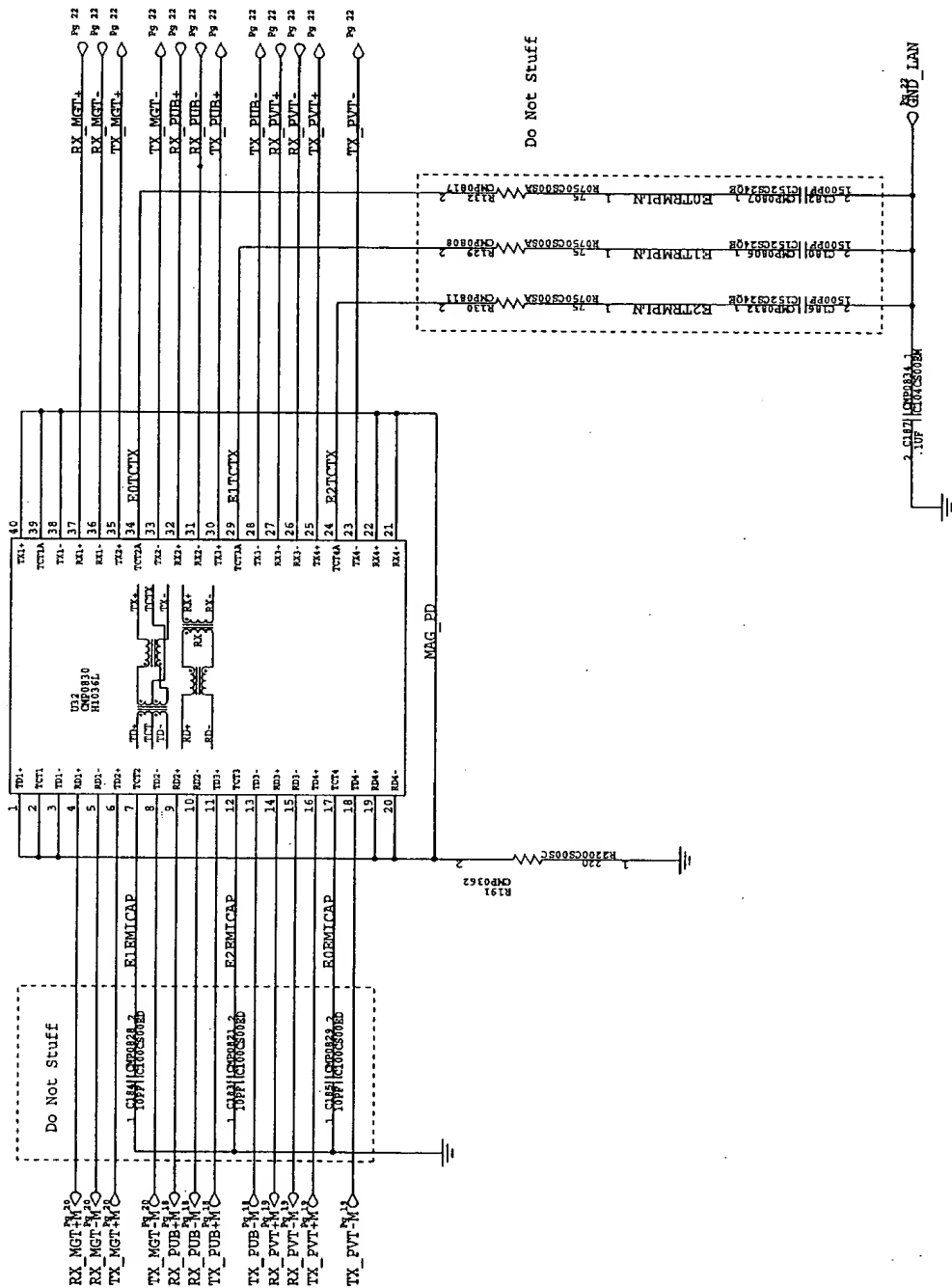






MID PLANE SIDE

82559 SIDE

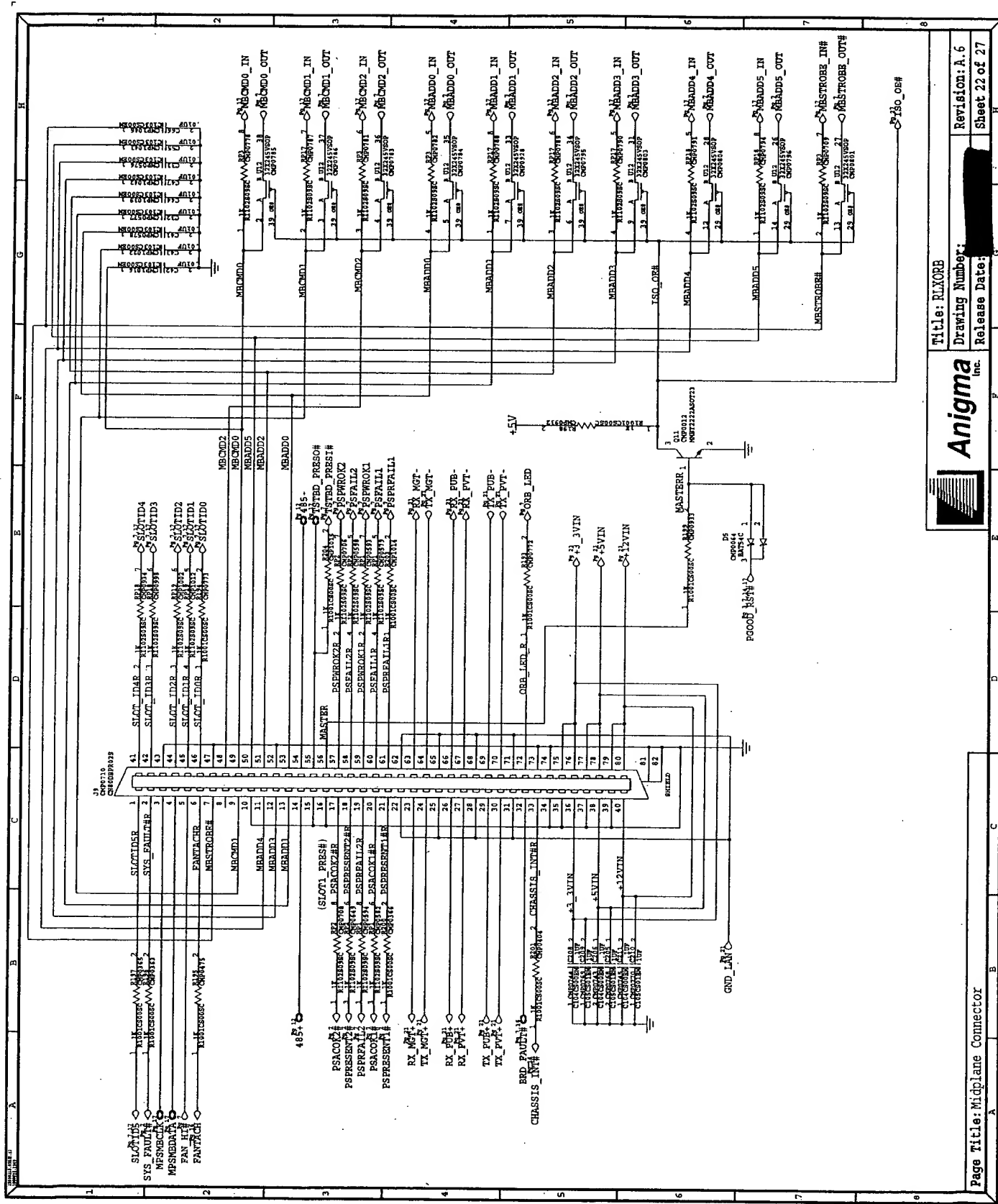


Do Not Stuff

Title: RLX08B  
Drawing Number:  
Release Date:

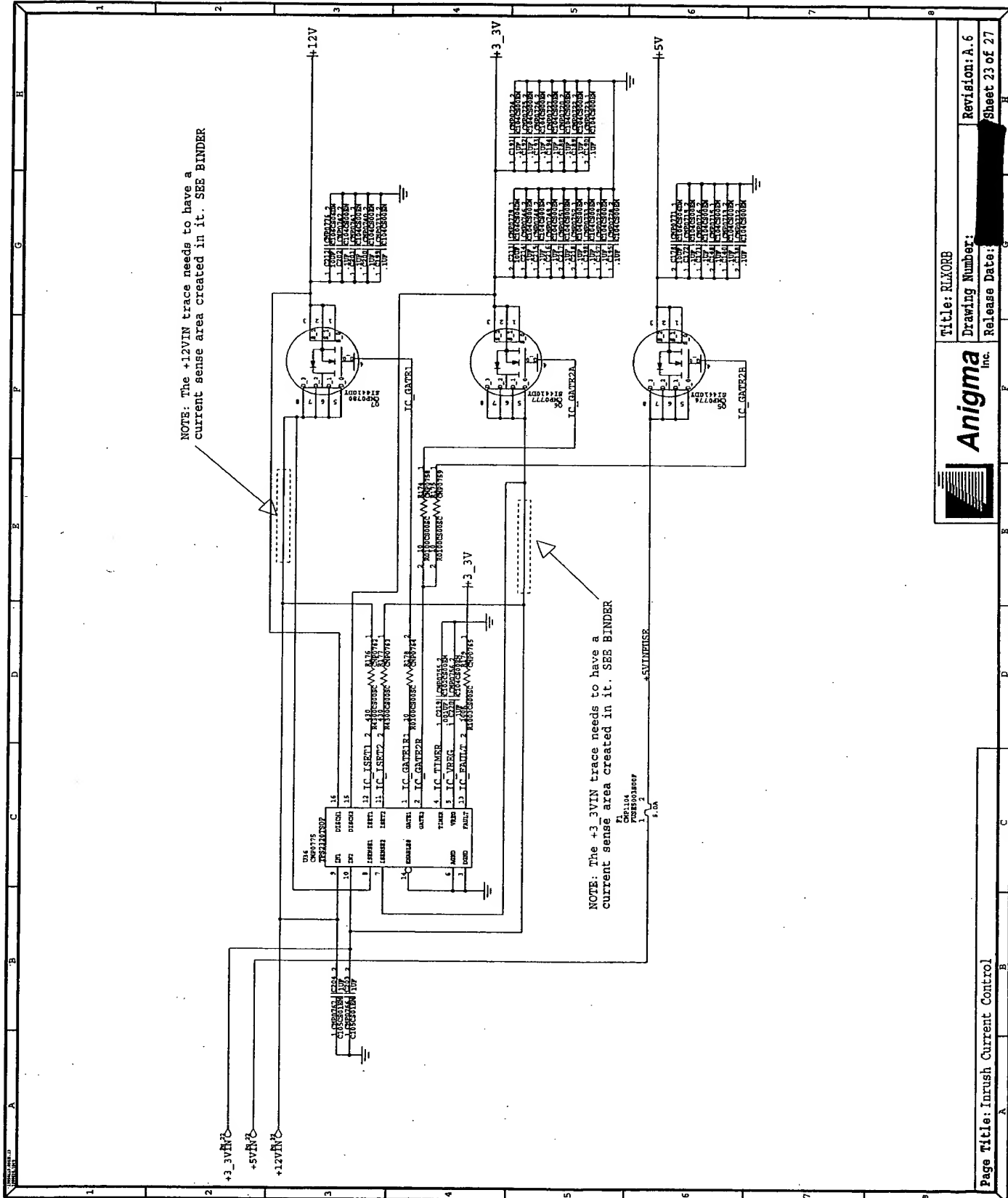
Anigma Inc.

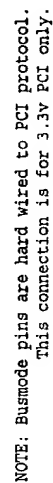
Revision: A.6  
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Title: RLXORB  
Drawing Number:  
Release Date:

Revision: A.6  
Sheet 22 of 27





## PMC CONNECTORS



**Anigma**<sup>Inc.</sup>

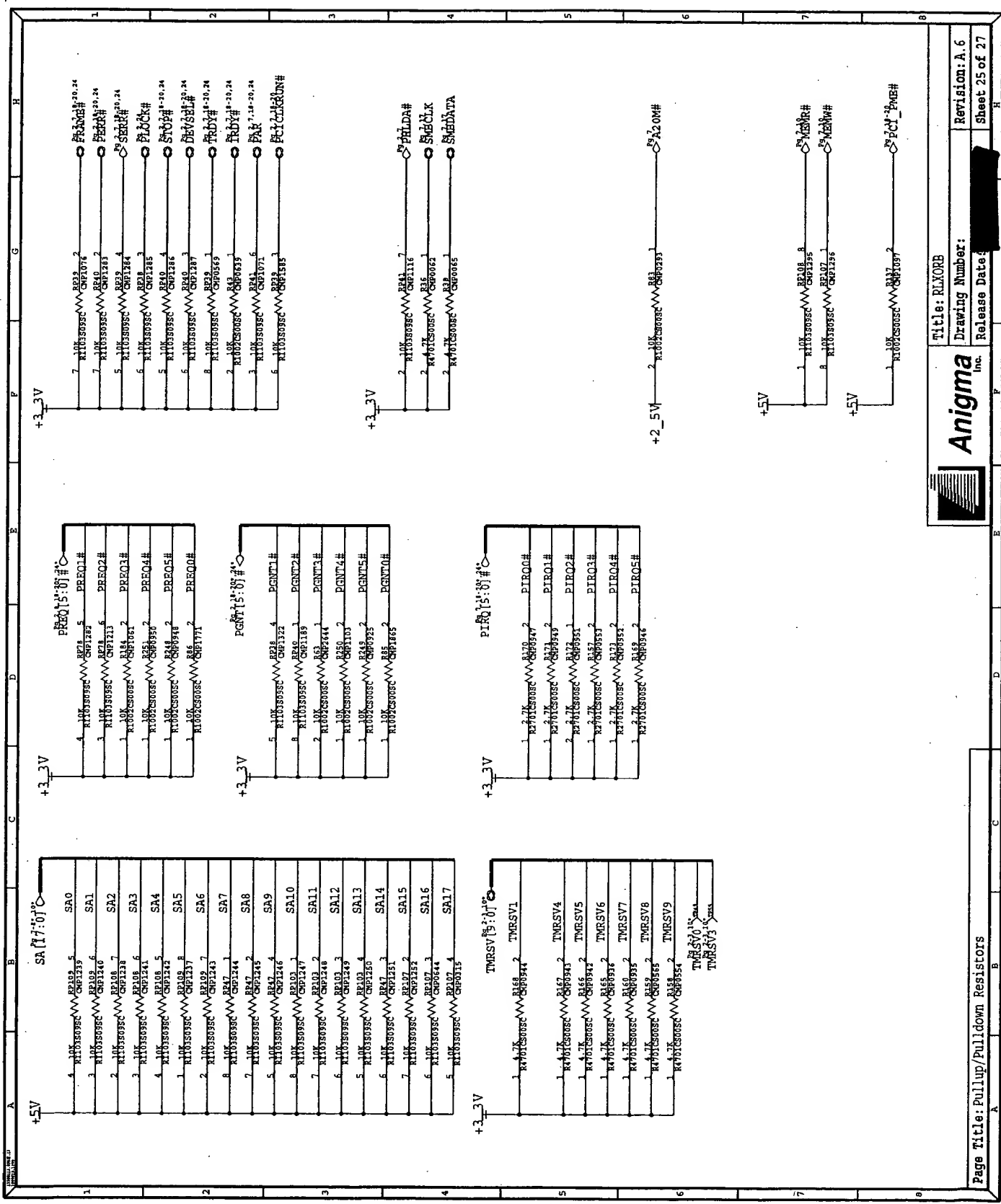
Title: RLXORB

**Drawing Number:**

**Release Date:**

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**Anigma**  
Inc.

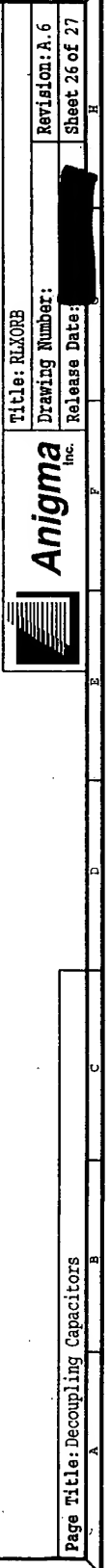
**Title:** RLXORB

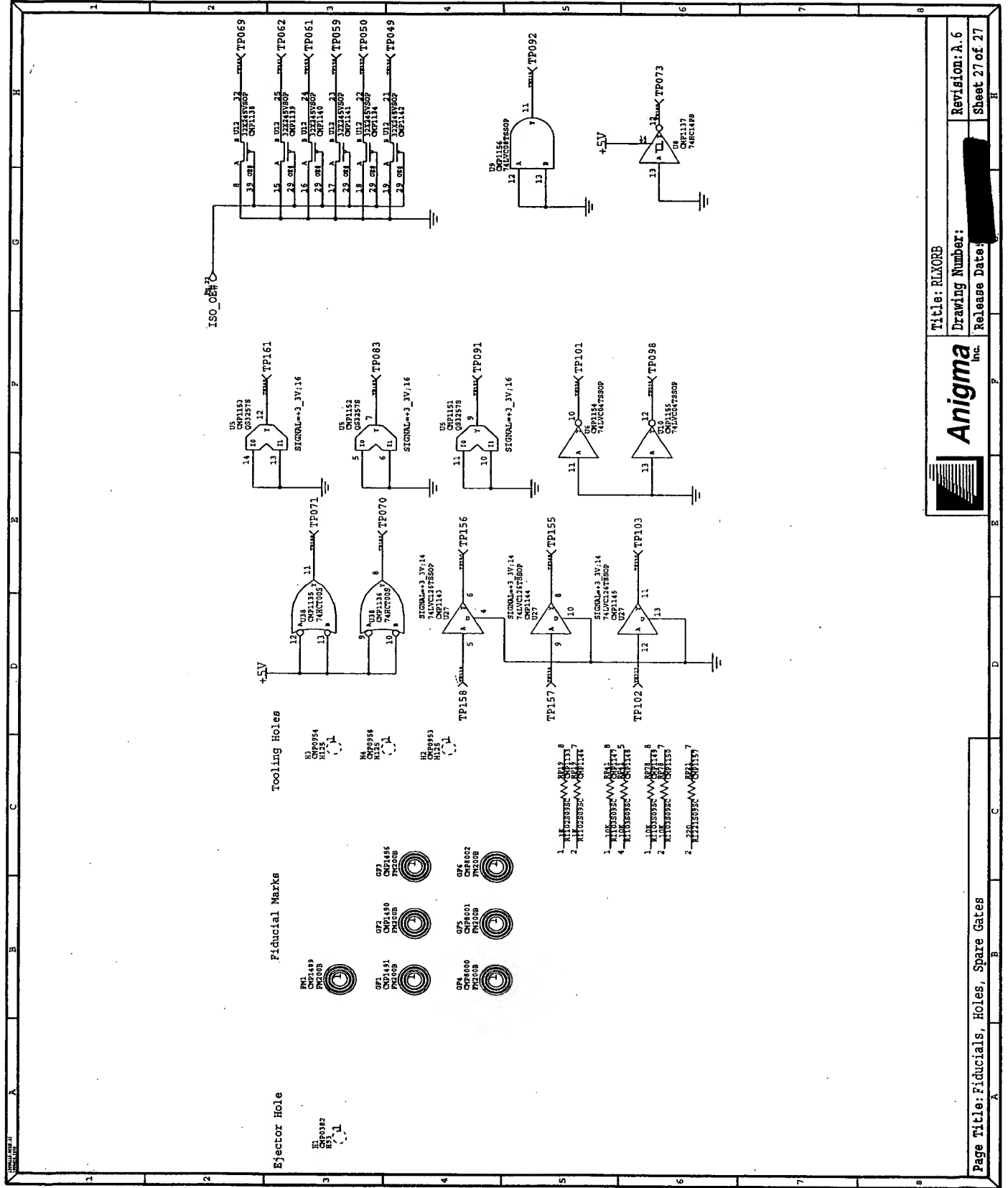
**Drawing Number:** [REDACTED]

**Release Date:** [REDACTED]

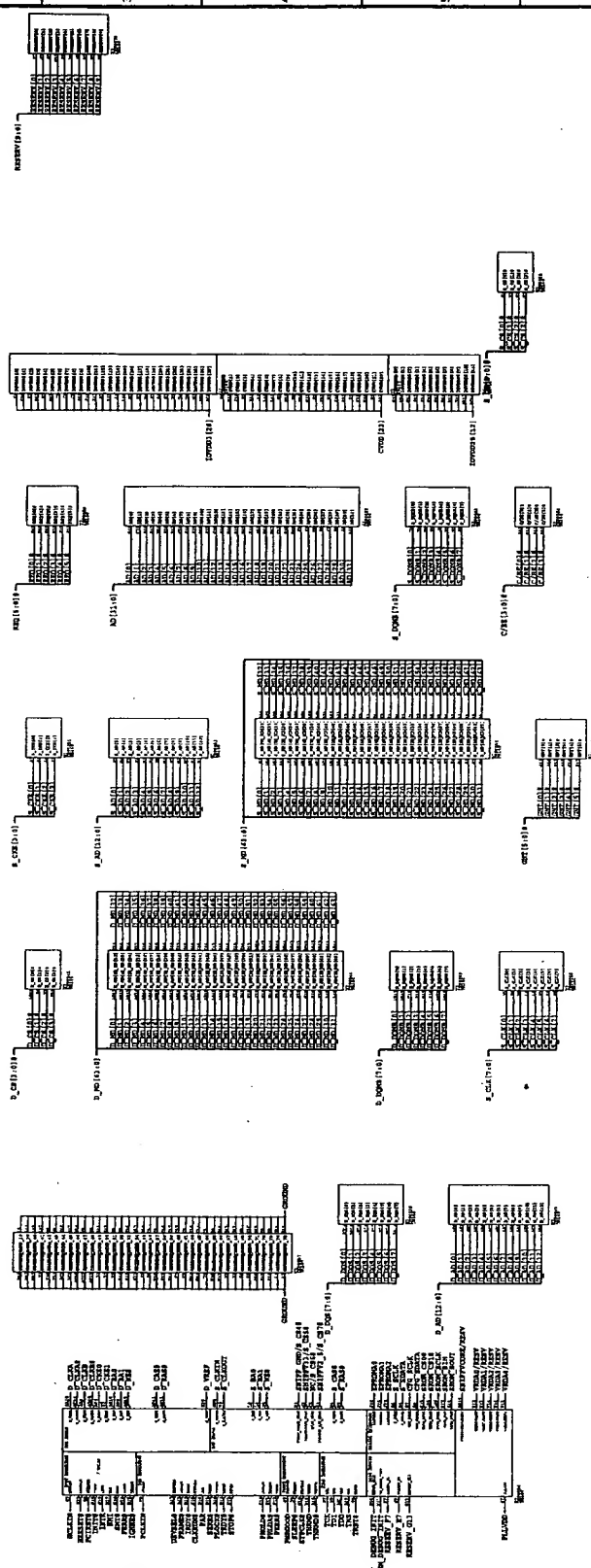
**Revision:** A.6

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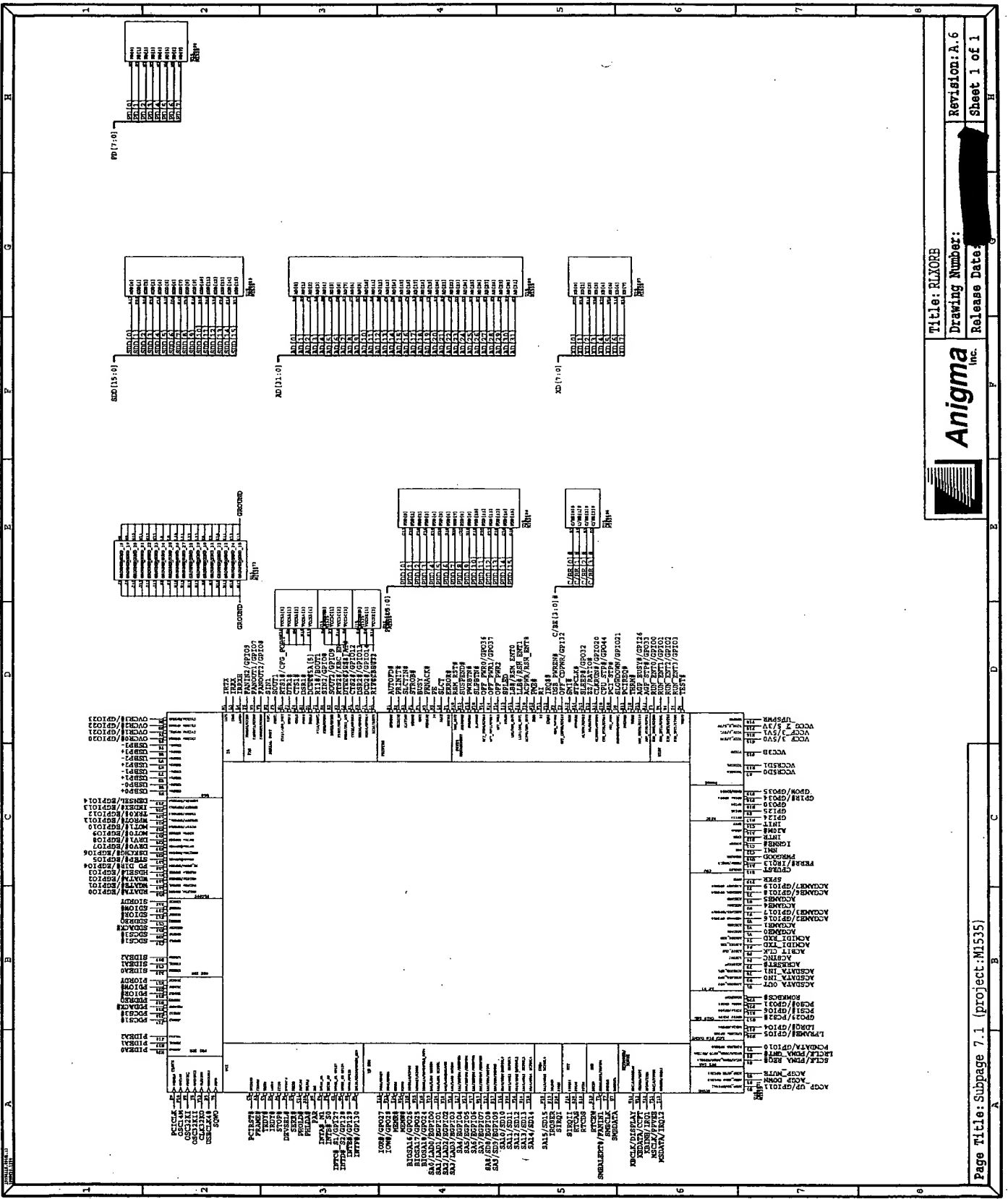












**Anigma**  
Inc.

Title: RLX08B

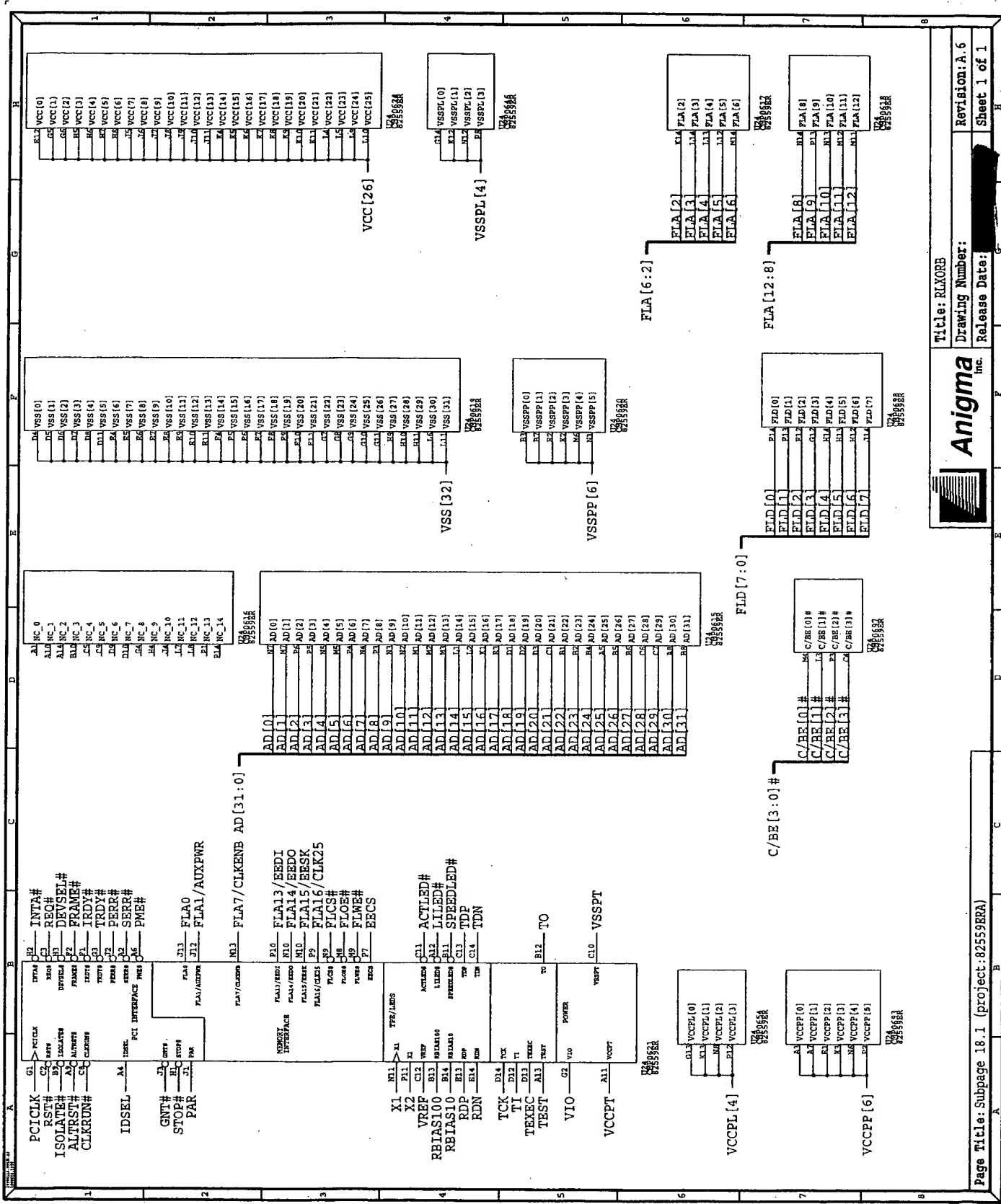
Revision: A.6


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Page Title: Subpage 7.1 (project: M1535)

Drawing Number:

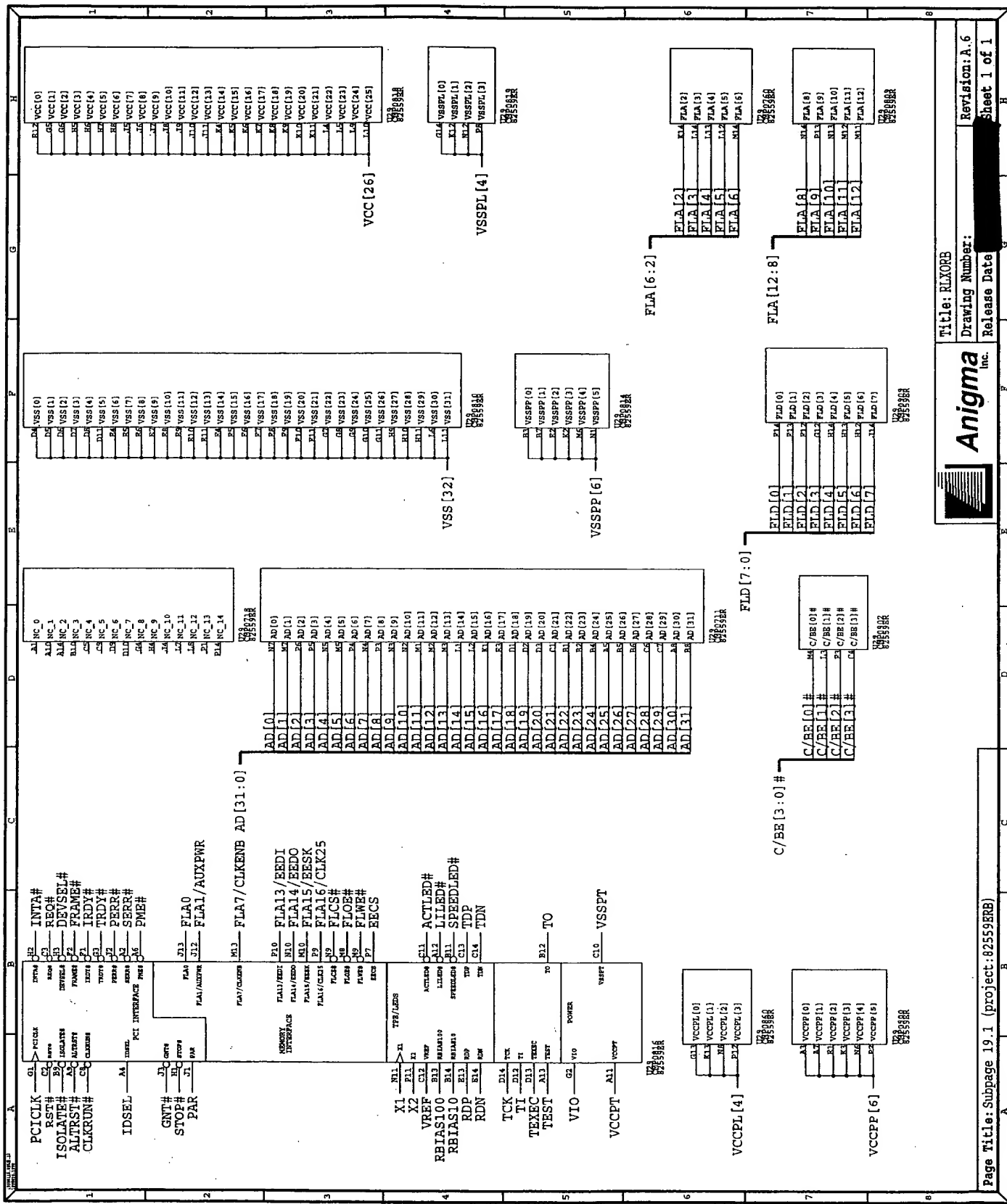
Release Date:



**Anigma**  
Inc.

Title: RLXORB  
Drawing Number: XXXXXXXXXX  
Release Date: XXXXXXXXXX

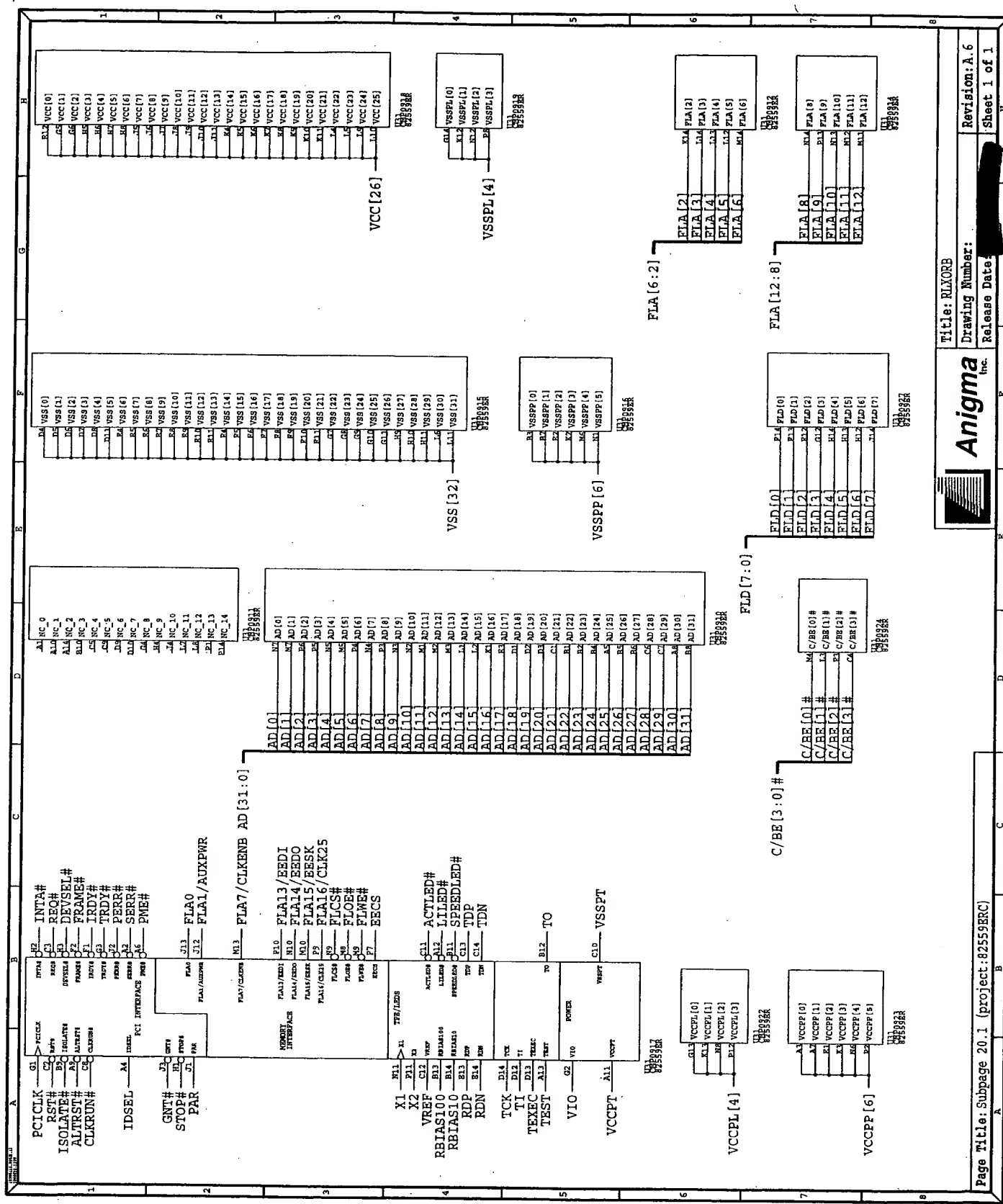
Revision: A.6  
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Title: RLX0RB  
Drawing Number: [Redacted]  
Release Date: [Redacted]



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